A New Balanced-to-Balanced Power Divider/Combiner

Bin Xia, Lin-Sheng Wu, *Member, IEEE*, and Junfa Mao, *Fellow, IEEE*

***Abstract*—In this paper, a new balanced-to-balanced power divider/combiner is proposed. By using matrix transformation, two three-port networks for the odd- and even-mode circuit models are deduced, based on the constraint rules of the mixed-mode S-parameters. In order to satisfy the two required scattering matrices simultaneously, the resistances of lumped elements, the characteristic impedances and electrical length of transmission lines are selected appropriately. Then, a planar microstrip structure is designed to realize the proposed balanced-to-balanced power divider/combiner with equal power division. The theoretical, simulated and measured results all show a good mixed-mode performance. In the measurement, the maximum differential-mode transmission coefficient is -3.2 dB, the best differential-mode isolation is 47.2 dB, and the fractional bandwidth of its operating band is approximately 20.8%.**

***Index Terms*—Balanced-to-balanced circuit, common mode, differential mode, matrix transformation, power divider/combiner.**

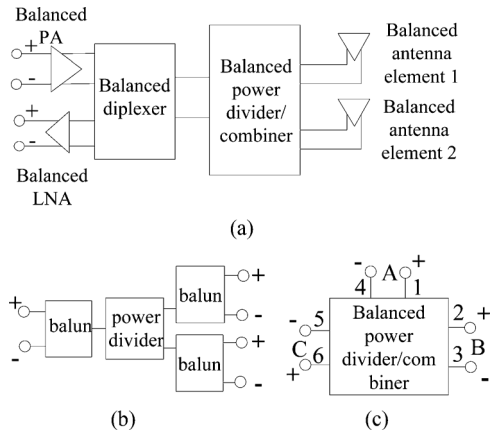

Fig. 1. (a) Fully balanced RF front-end. (b) Composite power divider/combiner composed of three baluns and a single-ended power divider/combiner. (c) Diagram of a balanced-to-balanced power divider/combiner.

I. Introduction

IT is well known that balanced RF circuits have more merits for modern communication systems than their single-ended counterparts. For example, balanced filters and diplexers show good common-mode suppression and high immunity to noise [1]–[4]; balanced and differentially driven antennas are not sensitive to the perturbations of ground plane and have wide impedance bandwidth and weak cross polarization [5]–[7]; balanced amplifiers have low noise, good input and output return losses, good linearity, and stability [8]–[10]; balanced mixers provide good port isolation and conversion efficiency [11], [12]; balanced oscillators can directly provide exact antiphase signals from an oscillator without the need for external baluns or resonators [13], [14].

Based on the balanced passive components and active devices, a fully balanced transceiver architecture can be constructed with higher immunity to the environmental noise compared with the single-ended signaling [15]. Fig. 1(a) shows a fully balanced RF front-end, where the output power of the balanced power amplifier (PA) is delivered to the antenna array with two balanced antenna elements and the received signal from the balanced antenna elements are transmitted to the input port of the balanced low-noise amplifier (LNA). It is easy to understand that a power divider/combiner is required in this front-end whose input and output ports are both balanced. The configuration shown in Fig. 1(b) can be used for this purpose, which is directly built up by three baluns and a single-ended power divider/combiner. However, the circuit size and in-band insertion loss may be relatively large.

Therefore, it is valuable to develop a balanced-to-balanced or differential-mode power divider/combiner, with its diagram shown in Fig. 1(c). The balanced ports A, B, and C are composed of the single-ended ports 1 and 4, ports 2 and 3, and ports 6 and 5, respectively. To the best of our knowledge, previous research on power divider/combiner has been mainly focused on single-ended components [16]–[18], and only a few balanced-to-balanced power dividers have been reported until now. In [19], a differential power divider is proposed by using shielded broadside-coupled striplines. However, the isolation between its differential output ports has not been considered in the design. Thus, the component cannot be used as a balanced-to-balanced power combiner.

In this paper, a new microstrip circuit is proposed to implement the balanced-to-balanced power divider/combiner. First, the requirements of the performance of the divider/combiner are described by the constraint rules of the mixed-mode S-parameters. Second, the two scattering matrices of the odd- and even-mode three-port networks are derived to fulfill the constraint rules. Then, a six-port circuit, built up of ideal transmission lines and lumped resistances, is proposed to realize the odd- and even-mode three-port networks. At last, the proposed

Manuscript received January 07, 2012; revised April 22, 2012; accepted May 02, 2012. Date of publication July 11, 2012; date of current version August 28, 2012. This work was supported by the National Basic Research Program of China under Grant 2009CB320202.

B. Xia is with the Key Lab of Ministry of Education for Design and EMC of High-Speed Electronic Systems, Shanghai Jiao Tong University, Shanghai 200240, China, and also with the Zhenjiang Watercraft College, Zhenjiang City, 212003 Jiangsu Province, China.

L.-S. Wu and J. Mao are with the Key Lab of Ministry of Education for Design and EMC of High-Speed Electronic Systems, Shanghai Jiao Tong University, Shanghai 200240, China (e-mail: jfmao@sjtu.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2012.2203926

balanced-to-balanced power divider/combiner is fabricated and measured to validate our design. The good performances of mixed-mode power division, reflection and isolation are given and discussed. Our proposed balanced-to-balanced power divider/combiner can provide equal differential-mode power dividing/combining, good port isolation, common-mode rejection and no convention between the differential- and common modes simultaneously within a single component for the first time.

II. Constraint Rules of a Balanced-to-Balanced Power Divider/Combiner

A. Mixed-Mode Scattering Matrix of a Balanced-to-Balanced Power Divider/Combiner

As shown in Fig. 1(c), the proposed balanced-to-balanced power divider/combiner is a six-port component. Let $[V^R]$ and $[V^I]$ represent the normalized reflected and incident wave vectors, respectively, and $[S^{std}]$ represents the 6×6 scattering matrix of the proposed balanced-to-balanced power divider/combiner. The relationship between them can be written by

$$\left[V^R\right] = \left[S^{std}\right]\left[V^I\right]. \tag{1}$$

Assume that the proposed balanced-to-balanced power divider/combiner is a reciprocal six-port network. Then we have $S_{mn} = S_{nm}$, where S_{mn} and S_{nm} are the elements of $[S^{std}]$, and $m, n = 1, \ldots, 6$. In our design, the power divider/combiner has an equal power division, which means ports 1–3 are symmetric to ports 4–6, i.e., $[S^{std}]$ can be written by

$$\left[S^{std}\right] = \begin{bmatrix} [S_U] & [S_D] \\ [S_D] & [S_U] \end{bmatrix} = \begin{bmatrix} a & b & c & d & e & f \\ b & g & h & e & i & j \\ c & h & k & f & j & l \\ d & e & f & a & b & c \\ e & i & j & b & g & h \\ f & j & l & c & h & k \end{bmatrix} \tag{2}$$

where $[S_{\mathrm{U}}]$ and $[S_{\mathrm{D}}]$ are both 3×3 submatrices.

When the balanced ports are defined as shown in Fig. 1(c), the mixed-mode scattering matrix $[S^{mm}]$ can be obtained from $[S^{std}]$ by using the matrix transformation [20]. We have

$$[S^{mm}] = \begin{bmatrix} [S^{dd}] & [S^{dc}] \\ [S^{cd}] & [S^{cc}] \end{bmatrix} \tag{3a}$$

$$\left[S^{dd}_{3\times3}\right] = \frac{1}{2}\begin{bmatrix} 2(a-d) & b-c-e+f & b-c-e+f \\ b-c-e+f & g-2h+k & -i+2j-l \\ b-c-e+f & -i+2j-l & g-2h+k \end{bmatrix} \tag{3b}$$

$$\left[S^{dc}_{3\times3}\right] = \frac{1}{2}\begin{bmatrix} 0 & b+c-e-f & -b-c+e+f \\ b-c+e-f & g-k & i-l \\ -b+c-e+f & -i+l & -g+k \end{bmatrix} \tag{3c}$$

$$\left[S^{cd}_{3\times3}\right] = \frac{1}{2}\begin{bmatrix} 0 & b-c+e-f & -b+c-e+f \\ b+c-e-f & g-k & -i+l \\ -b-c+e+f & i-l & -g+k \end{bmatrix} \tag{3d}$$

$$\left[S^{cc}_{3\times3}\right] = \frac{1}{2}\begin{bmatrix} 2(a+d) & b+c+e+f & b+c+e+f \\ b+c+e+f & g+2h+k & i+2j+l \\ b+c+e+f & i+2j+l & g+2h+k \end{bmatrix} \tag{3e}$$

where the 3×3 submatrices $[S^{dd}]$ and $[S^{cc}]$ indicate the differential-mode and common-mode scattering matrices, respectively, $[S^{dc}]$ indicates the conversion from common mode to differential mode, and $[S^{cd}]$ indicates the conversion from differential mode to common mode. It is found that

$$\left[S^{dd}_{3\times3}\right] = \left[S^{dd}_{3\times3}\right]^T \tag{4a}$$

$$\left[S^{cd}_{3\times3}\right] = \left[S^{dc}_{3\times3}\right]^T \tag{4b}$$

$$\left[S^{cc}_{3\times3}\right] = \left[S^{cc}_{3\times3}\right]^T \tag{4c}$$

where T means the transpose of a matrix.

B. Constraint Rules of the Proposed Balanced-to-Balanced Power Divider/Combiner

In order to provide ideal performance of balanced power dividing and combining, the proposed component should satisfy the following constraint rules.

1) When a differential-mode signal is fed into the balanced port A, no differential-mode power should be reflected, i.e., $a - d = 0$, no power should be converted to the common-mode output at the balanced ports B and C, i.e., $b+c-e-f = 0$, and the differential-mode output at the balanced ports B and C should satisfy $|b - c - e + f| = \sqrt{2}$. From (3d), we can also find that no power is converted to the common-mode reflection of the balanced port A in this case.
2) When a common-mode noise goes into the balanced port A, no noise in the form of differential mode or common mode should be outputted at the balanced ports B and C, i.e., $b - c + e - f = 0$ and $b + c + e + f = 0$. From (3c), it can be found that no power is converted to the differential-mode reflection of the balanced port A in this case.
3) When the differential-mode signal is fed into the balanced port B (C), no power should be converted into the differential-mode and common-mode reflection, i.e., $g-2h+k = 0$ and $g - k = 0$, and no power should be transmitted to the balanced port C (B) in the form of differential mode or common mode, i.e., $-i + 2j - l = 0$ and $i - l = 0$.
4) When a common-mode noise goes into the balanced port B (C), no power is reflected in the form of differential mode, i.e., $g - k = 0$, and no noise in the form of differential mode or common mode should be outputted at the balanced port A and C (B), i.e., $b + c - e - f = 0$, $-i + l = 0$, $b + c + e + f = 0$ and $i + 2j + l = 0$.

Based on the above constraint rules, the following equations are derived:

$$a = d \tag{5a}$$

$$b = -c = -e = f \tag{5b}$$

$$|b| = \frac{\sqrt{2}}{4} \tag{5c}$$

$$g = h = k \tag{5d}$$

$$i = j = l = 0 \tag{5e}$$

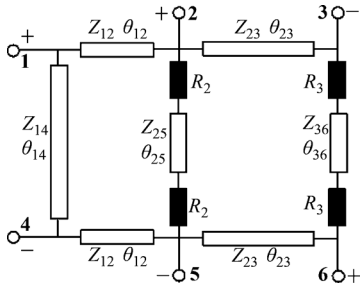

Fig. 2. Proposed balanced-to-balanced power divider/combiner circuit model.

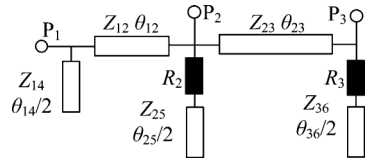

Fig. 3. Even-mode circuit model of the proposed balanced-to-balanced power divider/combiner.

C. Odd- and Even-Mode Scattering Matrices of the Proposed Balanced-to-Balanced Power Divider/Combiner

Since the proposed six-port balanced-to-balanced power divider/combiner is a symmetric circuit, the odd-/even-mode method is applied for analysis. For even-mode excitation, we have $v_1^I = v_4^I$, $v_2^I = v_5^I$, $v_3^I = v_6^I$, where v_n^I is the normalized incident wave of the nth single-ended port. For odd-mode excitation, we have $v_1^I = -v_4^I$, $v_2^I = -v_5^I$, and $v_3^I = -v_6^I$. Then, the even-mode and odd-mode scattering matrices are calculated by

$$[S_e] = [S_U] + [S_D] \tag{6a}$$

$$[S_o] = [S_U] - [S_D]\,. \tag{6b}$$

Substituting the constraint rules of (5) into (6), $[S_e]$ and $[S_o]$ can be obtained by

$$[S_e] = \begin{bmatrix} 2a & 0 & 0 \\ 0 & g & g \\ 0 & g & g \end{bmatrix} \tag{7a}$$

$$[S_o] = \begin{bmatrix} 0 & 2b & -2b \\ 2b & g & g \\ -2b & g & g \end{bmatrix}. \tag{7b}$$

If we can find a symmetric six-port circuit whose even-mode and odd-mode scattering matrices have the forms of (7a) and (7b), respectively, a balanced-to-balanced power divider/combiner will be achieved.

III. Realization of the Balanced-to-Balanced Power Divider/Combiner

In order to realize a balanced-to-balanced power divider/combiner based on the above theory, the circuit shown in Fig. 2 is utilized. It consists of seven transmission lines and four resistances, where $\theta_{14} = \theta_{25} = \theta_{36} = \pi$ at the central frequency f_0.

A. Even-Mode Circuit Model

As shown in Fig. 3, it is easy to obtain the even-mode circuit model from Fig. 2, which is a three-port network with each port matched to Z_0. Obviously, we have $[S_e]_{11} = -1$ and $[S_e]_{12} = [S_e]_{13} = [S_e]_{21} = [S_e]_{31} = 0$ at f_0.

The two-port ABCD-matrix between the ports 2 and 3 for the even-mode circuit model can be calculated by

$$\begin{bmatrix} A_e^{23} & B_e^{23} \\ C_e^{23} & D_e^{23} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{j\cot\theta_{12}}{Z_{12}} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{R_2} & 1 \end{bmatrix} \bullet \begin{bmatrix} \cos\theta_{23} & jZ_{23}\sin\theta_{23} \\ \frac{j\sin\theta_{23}}{Z_{23}} & \cos\theta_{23} \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{R_3} & 1 \end{bmatrix}. \tag{8}$$

Then, we have

$$A_e^{23} = \cos\theta_{23} + jZ_{23}\frac{1}{R_3}\sin\theta_{23} \tag{9a}$$

$$B_e^{23} = jZ_{23}\sin\theta_{23} \tag{9b}$$

$$C_e^{23} = \left[\left(-\frac{j\cot\theta_{12}}{Z_{12}} + \frac{1}{R_2}\right)\cos\theta_{23} + \frac{j\sin\theta_{23}}{Z_{23}}\right] + \frac{1}{R_3}\left[\left(-\frac{j\cot\theta_{12}}{Z_{12}} + \frac{1}{R_2}\right)jZ_{23}\sin\theta_{23} + \cos\theta_{23}\right] \tag{9c}$$

$$D_e^{23} = \left(-\frac{j\cot\theta_{12}}{Z_{12}} + \frac{1}{R_2}\right)jZ_{23}\sin\theta_{23} + \cos\theta_{23}. \tag{9d}$$

The S-parameters between the ports 2 and 3 for the even-mode model can be calculated from the corresponding ABCD matrix [21], and the derived even-mode S-parameters must meet the requirement of (7a). Therefore, the following equations should be satisfied:

$$A_e^{23} = D_e^{23} \tag{10a}$$

$$\frac{B_e^{23}}{Z_0} - C_e^{23}Z_0 = 2. \tag{10b}$$

Substituting (9) into (10), we will have

$$\cot\theta_{12}\sin\theta_{23} = 0 \tag{11a}$$

$$\left(\frac{1}{R_2} - \frac{1}{R_3}\right)\sin\theta_{23} = 0 \tag{11b}$$

$$\cos\theta_{23} = -\frac{2}{Z_0}\frac{R_2R_3}{R_2+R_3} \tag{11c}$$

$$\left(\frac{Z_{23}}{Z_0} - \frac{Z_0}{Z_{23}} - \frac{Z_0Z_{23}}{R_2R_3}\right)\sin\theta_{23} = 0. \tag{11d}$$

B. Odd-Mode Circuit Model

From Fig. 2, we can also obtain the odd-mode circuit model of the balanced-to-balanced power divider/combiner, as shown

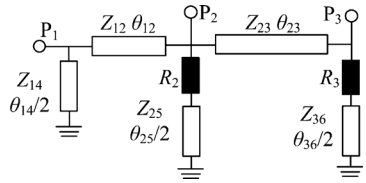

Fig. 4. Odd-mode circuit model of the proposed balanced-to-balanced power divider/combiner.

in Fig. 4. When the port 1 is terminated by Z_0, we can calculate the two-port ABCD-matrix between the ports 2 and 3 at f_0 by

$$\begin{bmatrix} A_o^{23} & B_o^{23} \\ C_o^{23} & D_o^{23} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{Z_{12}+jZ_0\tan\theta_{12}}{Z_{12}(Z_0+jZ_{12}\tan\theta_{12})} & 1 \end{bmatrix} \bullet \begin{bmatrix} \cos\theta_{23} & jZ_{23}\sin\theta_{23} \\ \frac{j\sin\theta_{23}}{Z_{23}} & \cos\theta_{23} \end{bmatrix}. \quad (12)$$

Then, the corresponding elements are given by

$$A_o^{23} = \cos\theta_{23} \quad (13a)$$

$$B_o^{23} = jZ_{23}\sin\theta_{23} \quad (13b)$$

$$C_o^{23} = \frac{(Z_{12}+jZ_0\tan\theta_{12})\cos\theta_{23}}{Z_{12}(Z_0+jZ_{12}\tan\theta_{12})} + \frac{j\sin\theta_{23}}{Z_{23}} \quad (13c)$$

$$D_o^{23} = \frac{(Z_{12}+jZ_0\tan\theta_{12})\,jZ_{23}\sin\theta_{23}}{Z_{12}(Z_0+jZ_{12}\tan\theta_{12})} + \cos\theta_{23}. \quad (13d)$$

The scattering matrix between the ports 2 and 3 for the odd-mode circuit model is then calculated, which should meet the requirement of (7b). Then, the following equations are derived:

$$\sin\theta_{23} = 0 \quad (14a)$$

$$-\frac{Z_0(Z_{12}+jZ_0\tan\theta_{12})\cos\theta_{23}}{Z_{12}(Z_0+jZ_{12}\tan\theta_{12})} = 2. \quad (14b)$$

Combining (11) and (14), we can derive

$$\theta_{23} = n\pi, \qquad n = 1,3,5\ldots \quad (15a)$$

$$\frac{1}{R_2}+\frac{1}{R_3} = \frac{2}{Z_0} \quad (15b)$$

$$\theta_{12} = m\frac{\pi}{2}, \qquad m = 1,3,5\ldots \quad (15c)$$

$$Z_{12} = \frac{\sqrt{2}Z_0}{2}. \quad (15d)$$

It should be indicated that the above equations is valid only at the central frequency.

According to (15), the three-port scattering matrices of the even- and odd-mode circuit models at f_0 are derived as

$$[S_e] = \begin{bmatrix} -1 & 0 & 0 \\ 0 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{1}{2} & -\frac{1}{2} \end{bmatrix} \quad (16a)$$

$$[S_o] = \begin{bmatrix} 0 & -j\frac{\sqrt{2}}{2} & j\frac{\sqrt{2}}{2} \\ -j\frac{\sqrt{2}}{2} & -\frac{1}{2} & -\frac{1}{2} \\ j\frac{\sqrt{2}}{2} & -\frac{1}{2} & -\frac{1}{2} \end{bmatrix}. \quad (16b)$$

Obviously, (16a) and (16b) are special cases of (7a) and (7b), respectively, where $b = -j\sqrt{2/4}$ and $a = g = -1/2$. Note that the value of b also satisfies (5c).

C. Scattering Matrix of the Balanced-to-Balanced Power Divider/Combiner

According to (6) and (16), the scattering matrix of the proposed balanced-to-balanced power divider/combiner can be deduced at the central frequency f_0 by

$$[S_U] = \begin{bmatrix} -\frac{1}{2} & -j\frac{\sqrt{2}}{4} & j\frac{\sqrt{2}}{4} \\ -j\frac{\sqrt{2}}{4} & -\frac{1}{2} & -\frac{1}{2} \\ j\frac{\sqrt{2}}{4} & -\frac{1}{2} & -\frac{1}{2} \end{bmatrix} \quad (17a)$$

$$[S_D] = \begin{bmatrix} -\frac{1}{2} & j\frac{\sqrt{2}}{4} & -j\frac{\sqrt{2}}{4} \\ j\frac{\sqrt{2}}{4} & 0 & 0 \\ -j\frac{\sqrt{2}}{4} & 0 & 0 \end{bmatrix}. \quad (17b)$$

The mixed-mode S-parameters are then calculated by

$$[S^{mm}] = \begin{bmatrix} 0 & j\frac{\sqrt{2}}{2} & j\frac{\sqrt{2}}{2} & 0 & 0 & 0 \\ j\frac{\sqrt{2}}{2} & 0 & 0 & 0 & 0 & 0 \\ j\frac{\sqrt{2}}{2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 \end{bmatrix}. \quad (18)$$

At f_0, it is seen from (18) that the proposed component provides equal power division without loss, perfect matching for each balanced port, and perfect isolation between the balanced ports B and C when differential-mode excitation is applied; it also provides total reflection and perfect isolation between balanced ports when common-mode excitation is applied; and it also guarantees that no conversion between differential and common modes will take place.

IV. Results and Discussion

A. Theoretical Results

From (15), the following can be found.

1) The characteristic impedances Z_{14}, Z_{25}, Z_{36}, and Z_{23} of the half-wavelength transmission lines can be selected arbitrarily, which will not affect the performance of the proposed power divider at the central frequency;
2) The loaded resistances R_2 and R_3 only need to satisfy (15b), whose detailed values will not affect the performance at the central frequency.

For miniaturization and simple design, the following design values are selected:

$$\theta_{14} = \theta_{23} = \theta_{25} = \theta_{36} = \pi \quad \text{at } f_0 \quad (19a)$$

$$\theta_{12} = \frac{\pi}{2} \quad \text{at } f_0 \quad (19b)$$

$$Z_{14} = Z_{23} = Z_{25} = Z_{36} = Z_x \quad (19c)$$

$$R_2 = R_3 = Z_0 = 50\,\Omega. \quad (19d)$$

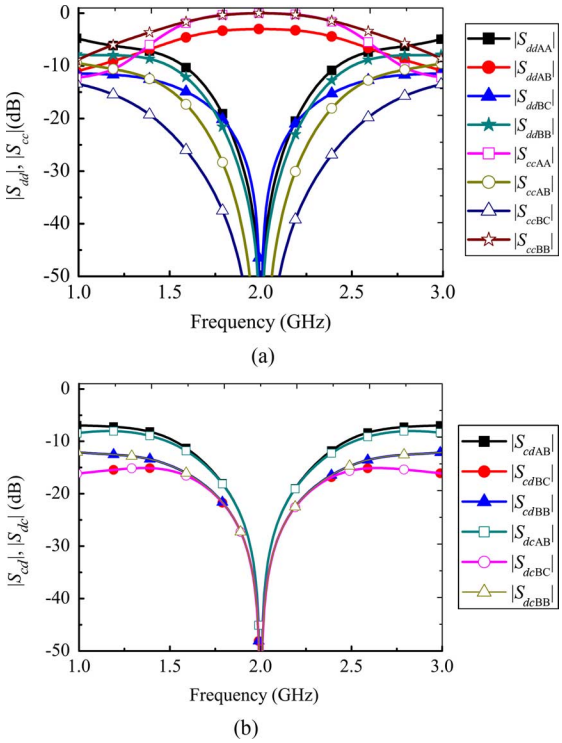

Fig. 5. Theoretical mixed-mode S-parameters of the balanced-to-balanced power divider/combiner prototype: (a) S_{dd} and S_{cc}; (b) S_{cd} and S_{dc}.

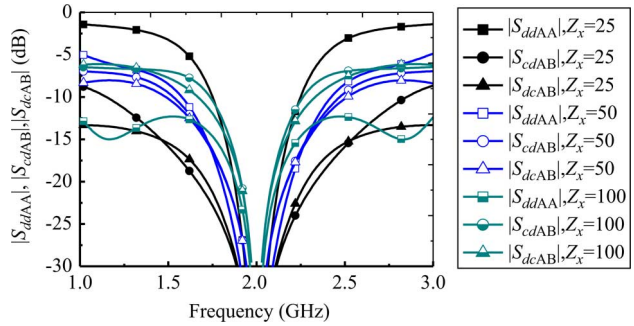

Fig. 6. Critical S-parameters of the balanced-to-balanced power divider/combiner to determine its bandwidth for different Z_x, where Z_x is in Ω.

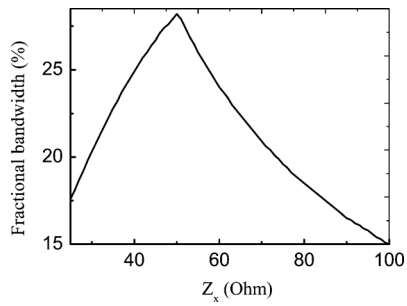

Fig. 7. Fractional bandwidth of the balanced-to-balanced power divider/combiner with variable Z_x.

Based on (19), a prototype of the balanced-to-balanced power divider/combiner is designed with the central frequency of $f_0 = 2.0$ GHz . We set $Z_{14} = Z_{25} = Z_{36} = Z_{23} = 50\ \Omega$. The theoretical results are shown in Fig. 5, where the lossless transmission lines and ideal lumped resistors are used. Since the balanced ports B and C are symmetric, some mixed-mode S-parameters are omitted. Note that the S-parameters are identified as S_{ddAB}, which refers to the differential to differential mode between ports B and A in Fig. 1, and the other S-parameters use a similar naming system. Note that the value of $S_{cd\mathrm{AA}} = S_{dc\mathrm{AA}}$ is always equal to zero due to the symmetry between ports 1 and 4, and the corresponding theoretical curves are not plotted in Fig. 5(b).

As shown in Fig. 5, the differential-mode transmission coefficient and the common-mode reflection coefficient reach their maximum of $|S_{dd\mathrm{AB}}| = -3.01$ dB and $|S_{cc\mathrm{AA}}| = |S_{cc\mathrm{BB}}| = 0$ dB at $f_0 = 2.0$, respectively. All the other mixed-mode S-parameters approach zero at f_0. Comparing the magnitudes of S_{cd} and S_{dc} in Fig. 5(b), we can find that the two groups of curves have almost the same values around the central frequency, which conforms to (4). It can be concluded that all the requirements of the proposed balanced-to-balanced power divider/combiner have been satisfied at the central frequency.

If the value of $|S_{dd\mathrm{AB}}|$ better than -4 dB and the values of $|S_{dd\mathrm{AA}}|$, $|S_{dd\mathrm{BB}}|$, $|S_{dd\mathrm{BC}}|$, $|S_{cc\mathrm{AB}}|$, $|S_{cc\mathrm{BC}}|$, $|S_{cd\mathrm{BB}}|$, $|S_{cd\mathrm{AB}}|$, $|S_{cd\mathrm{BC}}|$, $|S_{dc\mathrm{BB}}|$, $|S_{dc\mathrm{AB}}|$, $|S_{dc\mathrm{BC}}|$ all better than -15 dB should be satisfied simultaneously, an operating band can be achieved within 1.72 to 2.28 GHz, i.e., the fractional bandwidth of about 28%. It is also seen from Fig. 5 that the curves of $|S_{dd\mathrm{AA}}|$, $|S_{cd\mathrm{AB}}|$ and $|S_{dc\mathrm{AB}}|$ are critical to determine the bandwidth.

The influence of characteristic impedance Z_x on the fractional bandwidth is further studied numerically. Three group of curves are plotted in Fig. 6, with $Z_x = 25$, 50 and 100 Ω. The bandwidth limited by $|S_{cd\mathrm{AB}}|$ and $|S_{dc\mathrm{AB}}|$ under -15 dB decreases with the increasing of Z_x monotonically, while the bandwidth limited by $|S_{dd\mathrm{AA}}|$ under -15 dB first increases and then decreases with the increasing of Z_x. From Fig. 7, we can find that the proposed power divider has its maximum fractional bandwidth of 28% with $Z_x = 50\ \Omega$, when the curves of $|S_{dd\mathrm{AA}}|$, $|S_{cd\mathrm{AB}}|$ and $|S_{dc\mathrm{AB}}|$ intersect at -15 dB, as shown in Fig. 6. It should be pointed out that, if the operating bandwidth is measured by $|S_{dd\mathrm{AA}}|$, $|S_{cd\mathrm{AB}}|$, and $|S_{dc\mathrm{AB}}|$ better than -20 dB, the case of $Z_x = 44\ \Omega$ will provide the best fractional bandwidth of 19%.

At the central frequency, the half-wavelength transmission lines in the proposed circuit are a kind of phase inverter, and they can be replaced by any structure which can achieve 180° phase shift. Especially, if ideal phase inverters are utilized to replace the half-wavelength transmission lines, the proposed balanced-to-balanced power divider will have the same fractional bandwidth as a conventional single-ended Wilkinson power divider. When the phase inverters are realized by some physical structures, the bandwidth will also be limited by their performance. By utilizing other phase inverters with better broadband performance into the balanced-to-balanced power divider, wider operating band may be achieved than this work.

B. Simulated and Measured Results

As shown in Fig. 8, the prototype is realized with microstrip lines and surface-mounted lumped resistors and fabricated on an F4B substrate with the relative permittivity of $\varepsilon_r = 2.65$,

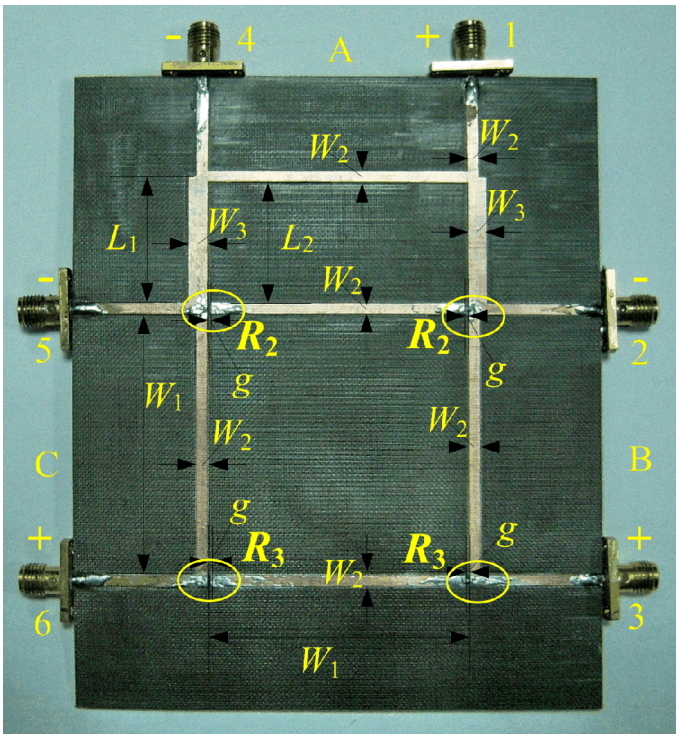

Fig. 8. Photograph of the balanced-to-balanced power divider/combiner prototype.

the loss tangent of $\tan\delta = 0.003$, and the thicknesses of $h = 0.73$ mm. Its critical dimensions are $W_1 = 50.76$ mm, $W_2 = 1.95$ mm, $W_3 = 3.28$ mm, $L_1 = 24.88$ mm, $L_2 = 23.91$ mm, and $g = 0.5$ mm. The total size is approximately $0.5 \times 0.75\ \lambda^2$.

The six-port S-parameters are simulated by the commercial software, Ansoft HFSS, and measured with the four-port vector network analyzer, Agilent E5071. Then, the mixed-mode S-parameters are extracted by using (3).

Fig. 9(a) and (b) shows a comparison between the simulated and measured transmission coefficients, reflection coefficients, and isolation between the balanced ports B and C for differential- and common-mode operation, respectively. Fig. 9(c) and (d) provides a comparison between the simulated and measured differential-to-common and common-to-differential mode conversions. Fig. 9(e) shows the magnified curves of $|S_{dd\mathrm{AB}}|$, $|S_{cc\mathrm{AA}}|$, and $|S_{cc\mathrm{BB}}|$. Good agreement is obtained.

The measured and simulated zeros of $|S_{dd\mathrm{AA}}|$, $|S_{dd\mathrm{BB}}|$, $|S_{dd\mathrm{BC}}|$, $|S_{cd\mathrm{AB}}|$, $|S_{cd\mathrm{BB}}|$, $|S_{cd\mathrm{BB}}|$, $|S_{cc\mathrm{BC}}|$, and $|S_{cc\mathrm{AB}}|$ all deviate from the designed central frequency of $f_0 = 2$ GHz, which is mainly caused by the discontinuities of microstrip lines and parasitic effect of the surface-mounted resistors. There is a little discrepancy between the curves in Fig. 9(c) and (d) due to the fabrication tolerance. The simulated $|S_{cd\mathrm{AA}}|$ and $|S_{dc\mathrm{AA}}|$ are always better than -50 dB, while the measured ones are better than -35 dB. The difference between the simulated and measured results is mainly caused by the nonideal symmetry of the fabricated prototype, which is also due to the tolerance of fabrication and the surface-mounted resistors.

In the measurements, the maximum differential-mode transmission coefficient of the prototype is $|S_{dd\mathrm{AB}}| = -3.2$ dB at 2.04 GHz, the best differential-mode isolation is 47.2 dB at 2.13 GHz, and the common-mode reflection coefficients of $|S_{cc\mathrm{AA}}|$

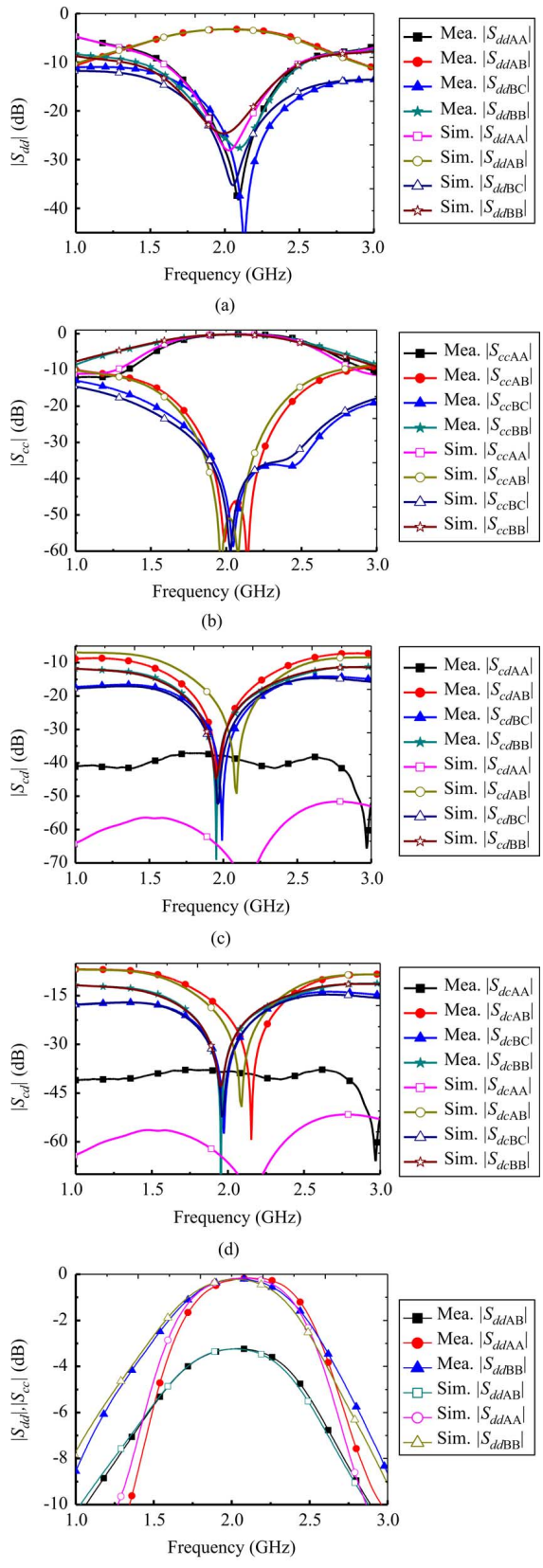

Fig. 9. Simulated and measured mixed-mode S-parameters of the prototype (a) $|S_{dd}|$, (b) $|S_{cc}|$, (c) $|S_{cd}|$, and (d) $|S_{dc}|$ and (e) the magnified curves of $|S_{dd\mathrm{AB}}|$, $|S_{cc\mathrm{AA}}|$ and $|S_{cc\mathrm{BB}}|$. Mea.: measured results. Sim.: simulated results.

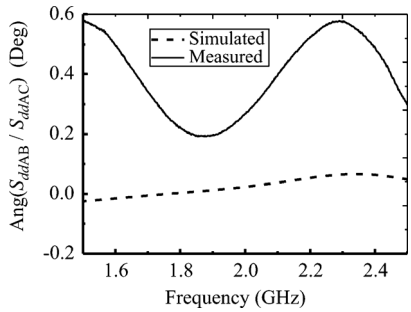

Fig. 10. Simulated and measured the phase differences between $S_{dd\mathrm{AB}}$ and $S_{dd\mathrm{AC}}$ of the prototype.

and $|S_{cc\mathrm{BB}}|$ reach their maximum of -0.16 and -0.2 dB at 2.11 and 2.06 GHz, respectively.

For the simulated results, the operating frequency band is from 1.80 to 2.30 GHz, with a fractional bandwidth of about 25%. The measured operating band is from 1.85 to 2.27 GHz, with a fractional bandwidth of about 20.8%, which is smaller than the theoretical bandwidth. This is mainly due to the frequency deviation, which is caused by fabrication tolerance.

Note that the referenced terminal of a differential pair can be defined freely in this circuit. As shown in Fig. 2, when we define the ports 2 (6) and (5) as the positive and negative terminals of balanced port B (C), respectively, the phase difference between the balanced ports B and C is close to zero. The simulated and measured phase differences of the two balanced ports are plotted in Fig. 10, which are better than 0.1° and 0.6° within the operating band, respectively. Obviously, if the ports 6 and 5 are defined as the negative and positive terminals of port C, respectively, while the referenced terminal definition of port B is kept unchanged, the proposed power divider will have an out-of-phase power division.

V. Conclusion

In this paper, a new concept of balanced-to-balanced power divider/combiner is proposed, which can replace three baluns and a single-ended power divider/combiner in a balanced RF front-end. First, the odd- and even-mode three-port networks of the new six-port component are analyzed by matrix transformation and derived according to the constraint rules of its mixed-mode S-parameters. Then, our proposed balanced-to-balanced power divider/combiner is built up with a combination of ideal transmission lines and resistances. Further, a prototype is realized by microstrip lines and surface-mounted lumped resistors to demonstrate our design. Good agreement has been obtained between the simulated and measured mixed-mode S-parameters. It is found that an equal power division and combining between two balanced ports is achieved with only the proposed component, which leads to simplified system architecture and low insertion loss. It can be expected that the new balanced-to-balanced power divider/combiner will be valuable in fully-balanced RF front-ends.

Acknowledgment

The authors would like to thank X. Yu and F. Niu, Agilent Technologies, Shanghai, China, for their assistance of measurement in this work.

References

[1] C.-H. Wu, C.-H. Wang, and C.-H. Chen, "Novel balanced coupled-line bandpass filters with common mode noise suppression," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 2, pp. 287–295, Feb. 2007.

[2] T.-B. Lim and L. Zhu, "A differential mode wideband bandpass filter on microstrip line for UWB application," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 10, pp. 632–634, Oct. 2009.

[3] J. Shi and Q. Xue, "Novel balanced dual-band bandpass filter using coupled stepped-impedance resonators," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 1, pp. 19–21, Jan. 2010.

[4] Q. Xue, J. Shi, and J.-X. Chen, "Unbalanced-to-balanced and balanced-to-unbalanced diplexer with high selectivity and common-mode suppression," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 11, pp. 2848–2855, Jan. 2011.

[5] R. Meys and F. Janssens, "Measuring the impedance of balanced antennas by an S-parameter method," *IEEE Antennas Propag. Mag.*, vol. 40, no. 6, pp. 65–68, Dec. 1998.

[6] Y.-P. Zhang, "Design and experiment on differentially driven microstrip antennas," *IEEE Trans. Antennas Propag*, vol. 55, no. 10, pp. 2701–2708, Oct. 2007.

[7] E. B. Kaldjob, B. Geck, and H. Eul, "Impedance measurement of properly excited small balanced antennas," *IEEE Antennas Wireless Propag. Lett.*, vol. 8, no. 6, pp. 65–68, Dec. 2009.

[8] R. S. Engelbrecht and K. Kurokawa, "A wideband low noise L-band balanced transistor amplifier," *Proc. IEEE*, vol. 53, no. 3, pp. 237–247, Mar. 1965.

[9] K. Kurokawa, "Design theory of balanced transistor amplifiers," *Bell Syst. Tech. J.*, vol. 44, pp. 1675–1698, Oct. 1965.

[10] J.-D. Jin and S. S. H. Hsu, "A 0.18-μm CMOS balanced amplifier for 24-GHz applications," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 440–445, Feb. 2008.

[11] S. A. Maas, "Novel single device balanced resistive HEMT mixers," *IEEE Trans. Microw. Theory Tech.*, vol. 43, no. 12, pp. 2863–2867, Dec. 1995.

[12] P.-Y. Chiang, C.-W. Su, S.-Y. Luo, R. Hu, and C.-F. Jou, "Wide-IF-band CMOS mixer design," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 4, pp. 831–840, Apr. 2010.

[13] K. W. Kobayashi, A. K. Oki, L. T. Tran, J. C. Cowles, A. Gutierrez-Aitken, F. Yamada, T. R. Block, and D. C. Streit, "A 108-GHZ InP-HBT monolithic push-push VCO with low phase noise and wide tuning bandwidth," *IEEE J. Solid-State Circuits*, vol. 34, no. 9, pp. 1225–1232, Sep. 1999.

[14] D. Baek, S. Ko, J.-G. Kim, D.-W. Kim, and S. Hong, "Ku-band InGaP-GaAs HBT MMIC VCOs with balanced and differential topologies," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 4, pp. 1353–1359, Apr. 2004.

[15] C.-H. Wang, Y.-H. Cho, C.-S. Lin, H. Wang, C.-H. Chen, D.-C. Niu, J. Yeh, C.-Y. Lee, and J. Chern, "A 60 GHZ transmitter with integrated antenna in 0.18 μm SiGe BiCMOS technology," in *IEEE Int. Solid-State Circuit Conf. Tech. Dig.*, Feb. 2006, pp. 186–187.

[16] Y. Wu, Y. Liu, Q. Xue, S. Li, and C. Yu, "Analytical design method of multiway dual-band planar power dividers with arbitrary power division," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 12, pp. 3832–3841, Dec. 2010.

[17] Y. Wu, Y. Liu, and Q. Xue, "An analytical approach for a novel coupled-line dual-band Wilkinson power divider," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 2, pp. 286–294, Feb. 2011.

[18] A. Genc and R. Baktur, "Dual- and triple-band Wilkinson power dividers based on composite right- and left-handed transmission lines," *IEEE Trans. Microw. Theory Tech.*, vol. 1, no. 3, pp. 327–334, Mar. 2011.

[19] J. W. May and G. M. Rebeiz, "A 40–50-GHz SiGe 1:8 differential power divider using shielded broadside-coupled striplines," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 7, pp. 1575–1581, Jul. 2008.

[20] D. E. Bockelman and W. R. Eisenstadt, "Combined differential and common mode scattering parameters: Theory and simulation," *IEEE Trans. Microw. Theory Tech.*, vol. 43, no. 7, pp. 1530–1539, Jul. 1995.

[21] J.-S. Hong and M. J. Lancaster, *Microstrip Bandpass Filters for RF/Microwave Applications*. New York: Wiley, 2001, ch. 1.

Bin Xia was born in 1976. He received the B.S. and M.S. degrees in electromagnetic fields and microwave technologies from PLA University of Science and Technology, Nanjing, China, in 2000, and 2003, respectively. He is currently working toward the Ph.D. degree in electromagnetic fields and microwave technologies at Shanghai Jiao Tong University, Shanghai, China.

From May 2003 to November 2005, he was an Engineer with the Institute of the General Staff Communication Design, Shenyang, China. Since November 2005, he has been a Lecturer with Zhenjiang Watercraft College, Zhenjiang, China. He serves as a reviewer for *Progress in Electromagnetics Research*.

Lin-Sheng Wu (S'09–M'10) was born in 1981. He received the B.S. degree in electronic and information engineering and M.S. and Ph.D. degrees in electromagnetic fields and microwave technologies from Shanghai Jiao Tong University, Shanghai, China, in 2003, 2006, and 2010, respectively.

From August to November 2010, he was a Research Fellow with the Department of Electrical and Computer Engineering, National University of Singapore. From February 2010 to January 2012, he held a post-doctoral position with Shanghai Jiao Tong University (SJTU), Shanghai, China. He is currently a Lecturer with the Key Laboratory of Ministry of Education of Design and Electromagnetic Compatibility of High Speed Electronic Systems, SJTU, where his present research interests are mainly focused on novel techniques for microwave integration and passive components. He is the author and coauthor of more than 50 technical papers.

Dr. Wu was a session co-chair of the Asia–Pacific Microwave Conference (APMC) and the IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS) in 2011. He is a reviewer of several international journals, including three IEEE transactions and letters.

Junfa Mao (M'92–SM'98–F'11) was born in 1965. He received the B.S. degree in radiation physics from the University of Science and Technology of National Defense, Changsha, China, in 1985, the M.S. degree in experimental nuclear physics from the Shanghai Institute of Nuclear Research, Shanghai, China, in 1988, and the Ph.D. degree in electronic engineering from Shanghai Jiao Tong University, Shanghai, in 1992.

Since 1992, he has been a Faculty Member with Shanghai Jiao Tong University, Shanghai, China, where he is currently a Chair Professor and the Executive Dean of the School of Electronic, Information and Electrical Engineering. He was a Visiting Scholar with the Chinese University of Hong Kong, Hong Kong, from 1994 to 1995, and a Postdoctoral Researcher with the University of California, Berkeley, from 1995 to 1996. He has authored or coauthored more than 190 journal papers (including 70 IEEE journal papers) and 120 international conference papers. He is a Chief Scientist with The National Basic Research Program (973 Program) of China, a project leader of the National Science Foundation for Creative Research Groups of China, and a Cheung Kong Scholar of the Ministry of Education, China. His research interests include the interconnect and package problem of integrated circuits and systems and analysis and design of microwave circuits.

Dr. Mao was the recipient of the National Natural Science Award of China in 2004, the National Technology Invention Award of China in 2008, and the Best Paper Award of the 2008 Symposium of APEMC in conjunction with the 19th International Symposium of Zurich EMC. He is an Associate Director of the Microwave Society of China Institute of Electronics, the 2007–2009 Chair of the IEEE Shanghai Section, and the 2009–2011 Chair of IEEE MTT Shanghai Chapter.