A Half-Mode Substrate Integrated Waveguide Ring for Two-Way Power Division of Balanced Circuit

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***Abstract*—A new balanced-to-balanced Gysel power divider (PD) is proposed for high-power applications, based on a half-mode substrate integrated waveguide (SIW) ring. The ring has a circumference of 2.5 λ_g, and one port is used for good isolation. The balanced-to-balanced component is easily designed by converting its single-ended counterpart. With the equivalent impedance defined by voltage and current of half-mode SIW, the initial geometry is quickly obtained. Good performance is achieved with our proposed PD, which has been demonstrated by its simulated and measured mixed-mode S-parameters.**

***Index Terms*—Balanced-to-balanced circuit, Gysel power divider (PD), half-mode substrate integrated waveguide (SIW), ring structure.**

I. Introduction

BALANCED circuits have been widely used in high-speed systems, because they can provide better immunity to environmental noises than their single-ended counterparts. Since additional baluns are no more required, many RF balanced filters are developed [1], [2]. When integrating a balanced filter with a differentially-driven antenna array in a balanced transmitter or receiver, a power divider (PD) operating with balanced input and balanced outputs is desired [3]. The authors have proposed a balanced-to-balanced PD/combiner for this new kind of application [4], which can divide the input power from a pair of balanced ports into two halves to another two pairs of balanced output ports. With balanced-to-balanced PDs, RF power can easily be assigned differentially.

On the other hand, substrate integrated waveguides (SIWs) have drawn much attention recently [5], due to their low loss, low cost, high power handling capability, easy integration, *etc*. Half-mode SIW is a type of miniaturized SIW [6]. PDs are realized with SIW and half-mode SIW [7]–[9]. One of their obvious merits is good power handling capability.

It is well known that the Gysel PD has advanced power handling capability [10], since its isolation between output ports is realized by grounded matched loads, instead of internal lumped resistors. If we extend the Gysel configuration into a balanced-to-balanced PD with the SIW technique, the power division with excellent power handling capability can be expected for balanced circuits.

In this letter, a new two-way balanced-to-balanced Gysel PD is proposed by using a half-mode SIW ring. Two ports are for the input balanced pair, four ports are for the two output balanced pairs, and the final one is for the matched load to achieve good isolation performance. The component is easily designed with a convenient conversion method from a single-ended Gysel PD. Its good performance has been demonstrated experimentally.

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II. Analysis and Design

A. Balanced-to-Balanced Gysel PD

A single-ended two-way Gysel PD is shown in Fig. 1(a), where a $\lambda_g/2$ transmission line is replaced by a phase inverter. For the design of a balanced-to-balanced circuit with the same function as a single-ended one, a simple method is to add a balun at each port and to divide the characteristic impedances and resistances of the circuit by two. The converted balanced-to-balanced Gysel PD is shown in Fig. 1(b). According to the perfect performance of ideal phase inverters, a ring topology can then be obtained for the two-way balanced-to-balanced Gysel PD by further simplifying the configuration, as shown in Fig. 1(c).

From Fig. 1(c), it is seen that if a uniform characteristic impedance is desired for the ring structure, we should have

$$R = \frac{Z_p}{2} \tag{1}$$

where Z_p is the port impedance, and R is the resistance of the isolation load. And the phase inverters may be realized by $\lambda_g/2$ transmission lines with an arbitrary characteristic impedance of Z_{pi}, where λ_g is the guided wavelength at the central frequency. In this design, the following condition is preferred:

$$Z_{pi} = \frac{\sqrt{2}Z_p}{2}. \tag{2}$$

Then, the balanced-to-balanced Gysel PD can be built up with a ring structure whose circumference is 2.5 λ_g.

B. Half-Mode SIW Ring Structure

In order to implement the balanced-to-balanced Gysel PD in Fig. 1(c) with excellent power handling capability, a 2.5 λ_g half-mode SIW ring is utilized in our design. The same as conventional metal waveguides, there are non-unique definitions of voltage, current and so-called equivalent impedance for a half-mode SIW, namely, Z_{VI}, Z_{PV} and Z_{PI} defined by voltage-

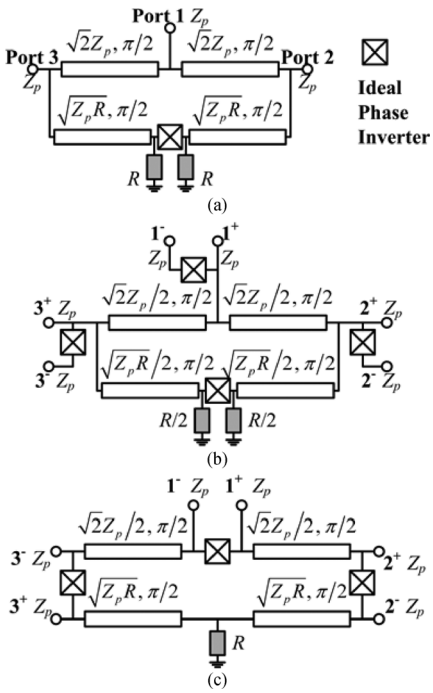

Fig. 1. Configurations of Gysel PDs: (a) a conventional single-ended one; (b) a balanced-to-balanced one directly converted from its single-ended counterpart; and (c) a simplified balanced-to-balanced one.

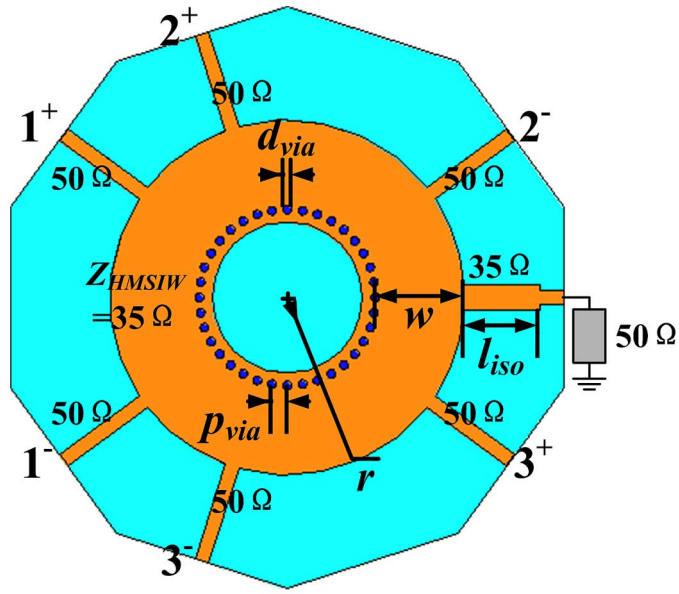

Fig. 2. Layout of our proposed balanced-to-balanced Gysel PD based on a half-mode SIW ring structure.

current, power-voltage and power-current, respectively. Based on the general definitions in a rectangular waveguide [11], the equivalent impedances of the dominant $\mathrm{TE}_{0.5,0}$-mode in a half-mode SIW can be written as

$$Z_{VI} = \frac{\pi}{2}\frac{h\eta_0}{\sqrt{\varepsilon_r w_e^2 - \left[\frac{c_0}{(4f)}\right]^2}} \tag{3}$$

$$Z_{PV} = 2\frac{h\eta_0}{\sqrt{\varepsilon_r w_e^2 - \left[\frac{c_0}{(4f)}\right]^2}} \tag{4}$$

$$Z_{PI} = \frac{\pi^2}{8}\frac{h\eta_0}{\sqrt{\varepsilon_r w_e^2 - \left[\frac{c_0}{(4f)}\right]^2}} \tag{5}$$

where w_e is the equivalent width of half-mode SIW considering the effects of metallic via-holes and open side [6], h is the height of half-mode SIW, η_0 is the intrinsic impedance of free space, c_0 is the wave velocity in vacuum, ε_r is the relative permittivity of substrate, and f is the operating frequency. When the substrate is preselected, all the equivalent impedances at a certain operating frequency f increase with the increasing of h and decrease with the increasing of w_e.

As shown in Fig. 2, the half-mode SIW ring is connected with six 50 Ω microstrip ports for convenient measurement. A 50 Ω load is used for isolation, and a quarter-wavelength microstrip line with the characteristic impedance of $\sqrt{2}Z_p/2 = 35\ \Omega$ is inserted to make the input impedance of the isolation load looked from the half-mode SIW ring be $R = Z_p/2 = 25\ \Omega$. The half-mode SIW ring should have an equivalent impedance of $Z_{HMSIW} = 35\ \Omega$. Since the TE-mode half-mode SIW is integrated with quasi-TEM-mode microstrip lines, it is very important to decide which equivalent impedance definition should be applied for the half-mode SIW in this case.

It should be indicated that the appropriate equivalent impedance of half-mode SIW looked from microstrip is related to their connection form or the transition between half-mode SIW and microstrip. Because the microstrip lines are directly connected to the open side of the half-mode SIW, where the electric field of the dominant TE-mode in half-mode SIW reaches its maximum, it is reasonable to assume that the equivalent voltage of half-mode SIW has the same value as that of microstrip lines. Further, around the open side, the traversal surface current on the top metal plane of the half-mode SIW is close to zero, while the longitudinal surface current reaches its maximum. Note that the equivalent current of waveguide is just defined by the longitudinal surface current. Therefore, the definition of Z_{VI} is preferred in this configuration.

In our design, the operating frequency of the component prototype is set to $f_0 = 5$ GHz. The Taconic RF-35A2 substrate is selected, whose relative permittivity and height are $\varepsilon_r = 3.5$ and $h = 0.762$ mm, respectively. The diameter and spacing of via-holes are $d_{via} = 1.0$ mm and $p_{via} = 1.8$ mm, respectively. It is obtained that $w = 10.2$ mm by using (3), together with the relationship between the equivalent width w_e and the physical width w of the half-mode SIW [6]. The guided wavelength in the half-mode SIW at f_0 is $\lambda_g = 49.0$ mm. Then, the radius of the ring structure is approximated to be $r = (5\lambda_g)/(4\pi) = 19.5$ mm.

III. Results and Discussion

Based on the initial geometric parameters in Section II.B, a balanced-to-balanced half-mode SIW Gysel PD is developed. The optimized physical width of waveguide is $w = 10.5$ mm,

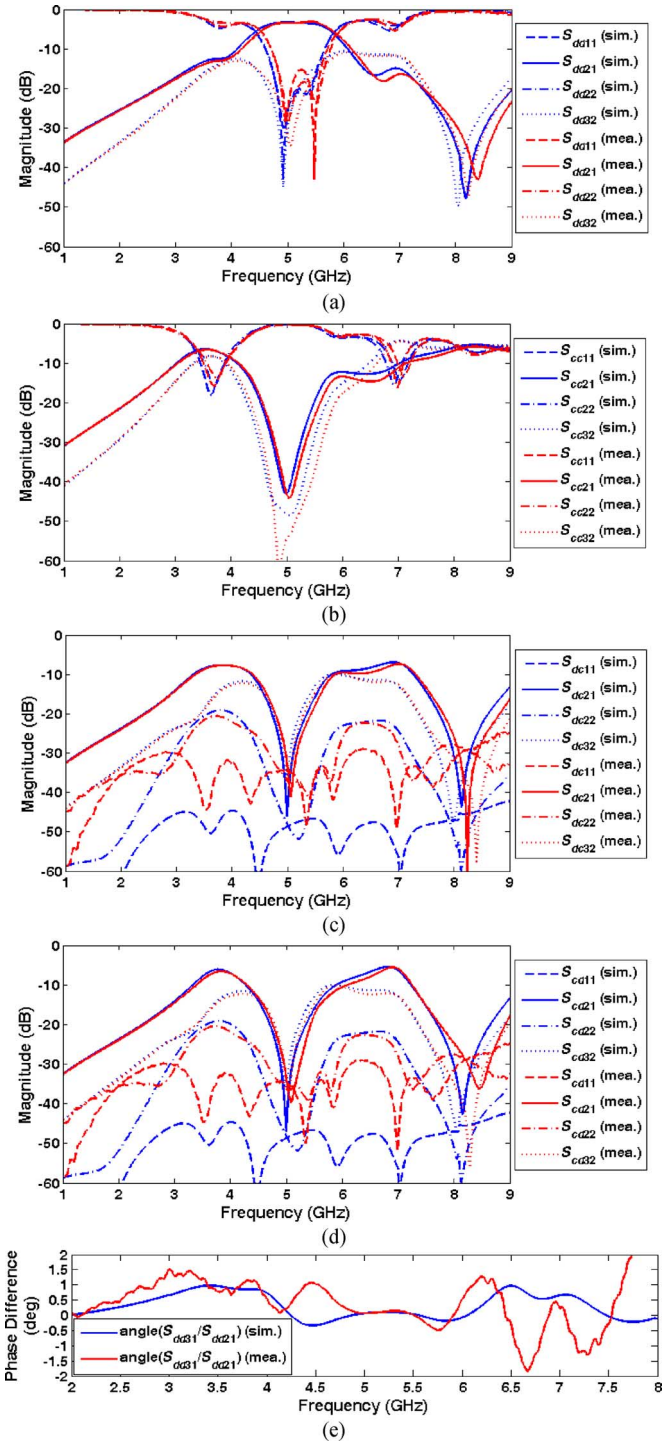

Fig. 3. Measured and simulated mixed-mode S-parameters of the balanced-to-balanced Gysel PD prototype: (a) S_{dd}; (b) S_{cc}; (c) S_{dc}; (d) S_{cd}; and (e) phase difference between S_{dd31} and S_{dd21}.

while the ring radius is $r = 20.85$ mm. The length of the quarter-wavelength 35 Ω microstrip line is $l_{iso} = 8.8$ mm. The overall size without ports is 50.5×41.7 mm^2.

The measured mixed-mode S-parameters of the prototype are plotted in Fig. 3, and the simulated ones are also obtained with ANSYS HFSS. All the measured results agree well with the simulated ones, except that the measured levels of $S_{dc(cd)11}$ and $S_{dc(cd)22}$ are about 15 dB higher than the simulated ones. The values of $S_{dc(cd)11}$ are very sensitive to the structure symmetry, which has been slightly disturbed by the fabrication tolerance. The discrepancy of $S_{dc(cd)22}$ may be caused by the impedance tolerance of microstrip lines at Ports 2^+ and 2^-. However, the measured $S_{dc(cd)11}$ are still below -30 dB, still good enough to suppress the conversion between differential and common modes at the balanced input pair. And the measured $S_{dc(cd)22}$ are still lower than -25 dB within the operating band.

The simulated and measured central frequency is 5.12 and 5.20 GHz, respectively. The little frequency shift is mainly due to the tolerance of relative permittivity. Both the simulated and measured central insertion losses of S_{dd21} are 3.4 (0.4+3.0) dB. The measured operating bandwidth is from 4.82 to 5.49 GHz, i.e., 13%, with S_{dd11}, S_{dd22}, S_{dd32}, S_{cc21}, S_{cc32} and all the S_{dc}- and S_{cd}-parameters below -15 dB. The measured in-band phase difference between S_{dd31} and S_{dd21} is within $\pm 0.2°$. The desired performance of the balanced-to-balanced Gysel PD has been implemented with the half-mode SIW ring structure.

IV. Conclusion

Based on a 2.5 λ_g half-mode SIW ring, a new two-way balanced-to-balanced Gysel PD is proposed for high-power applications. Its six ports are combined into three differential pairs, while a matched load is connected through a quarter-wavelength 35 Ω microstrip line to achieve good isolation. The component is easily developed, starting from its single-ended counterpart. And the initial geometric parameters are obtained analytically by using the voltage-current defined equivalent impedance of half-mode SIW. The good performance of the balanced-to-balanced PD has been demonstrated by its simulated and measured mixed-mode S-parameters.

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