High-Frequency Electrothermal Characterization of TSV-Based Power Delivery Network

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***Abstract*— In this paper, high-frequency electrothermal characteristics of the power delivery network (PDN) are investigated for through-silicon-via (TSV)-based 3-D ICs by utilizing a self-developed electrothermal co-simulation solver. The solver circularly solves the full-wave electromagnetic equation and the steady heat conduction equation using the finite-element method. The preconditioned biconjugate gradient method combined with the element-by-element approximate factorization method is employed to speed up the simulation and save memory cost. Based on the solver, the impacts of the excitation condition and dielectric loss tangent are analyzed for a one-chip power grid, while the influence of TSV location is studied for a two-chip PDN structure. In the modeling, both the conductor and dielectric losses are taken into account, and the temperature dependence of material parameters is treated appropriately. As results, PDN impedance and self-heating-induced temperature rise are emphatically analyzed in a wide frequency range, and the electric field and temperature distributions of several resonance modes are presented. The results would be beneficial for the design and thermal management of 3-D PDNs.**

***Index Terms*— 3-D IC, electrothermal co-simulation, finite-element method (FEM), power delivery network (PDN), through-silicon via (TSV).**

I. Introduction

With the technology advancing, a larger number of transistors with higher switching speed are integrated into a single chip, which increases the switching current containing different frequency components, and thereby causes severe voltage noise and dynamic power dissipation [1], [2]. What is more, in modern 3-D integration, where several chips are stacked and connected using through-silicon vias (TSVs), the switching current of each chip will be accumulated, thus making the current density much larger than their 2-D counterparts. Therefore, the switching-current-induced power and thermal integrity problems are critical in the design of the power delivery network (PDN), especially in 3-D ICs.

In order to effectively reduce the voltage noise, a PDN structure with low impedance from dc to high frequency is preferred. As the low-frequency impedance is mainly determined by the off-chip components (e.g., package and printed circuit board), we focus on the high-frequency PDN impedance in this paper for the chip-stack structure. In [3]–[9], the PDN impedance in high frequency has been well analyzed by circuit modeling methods, while the thermal effects were not considered.

It is well known that the thermal integrity becomes a major consideration in the PDN design for two contradictory reasons. First, 3-D integration increases power dissipation but lowers the heat removal. Second, the quick development of portable electronic devices requires the temperature rise to be as small as possible. Previous studies on the electrothermal properties of PDNs were carried out based on the equivalent circuit models [10]–[12], which may lack accuracy in the high-frequency region. Lu and Jin [13] performed the electrothermal co-simulation for PDNs and captured the transient responses under the Gaussian pulse. However, the PDN's electrothermal characteristics in a wide frequency band are out of consideration in these early works, but are the theme of this paper.

In this paper, an electrothermal solver is developed in a frequency domain based on the finite-element method (FEM) since it has an outstanding capacity in modeling complex structures and materials [14]–[19]. The co-simulation solver circularly solves the electric and heat boundary value problems. The vector wave equation based on Maxwell's equations is solved as the governing equation of the electric boundary value problem, while the steady heat conduction equation is solved as the governing equation of the thermal boundary value problem. The electromagnetic and thermal fields interact with each other, that is, the power dissipation caused by the electric field is taken as the heat source for the thermal problem, while the temperature rise changes the materials' parameters, which will in turn lead to updated solutions of the electric equations. By circularly solving the electric and thermal equations for convergence, the mutual interaction is successfully taken into account in the solver. Based on our co-simulation solver, the impedance value and the induced temperature rise are extracted at each frequency point. As the

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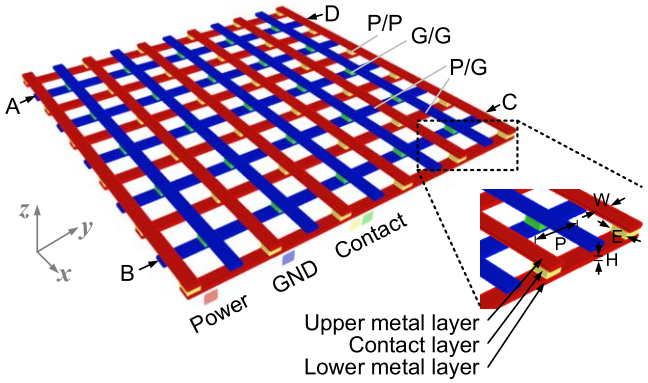

Fig. 1. Schematic of on-chip PDN grid. Four input ports are marked as A–D. P/P: overlap site between the power lines of two metal layers. G/G: overlap site between ground lines. P/G: overlap site between power and ground lines. Part of the structure is enlarged to show the detailed geometrical parameters.

TABLE I
GEOMETRICAL PARAMETERS

Parameter	Value (μm)
Wire width W	30
Wire height H	15
Wire pitch P	200
Wire length L	2030
Contact edge length E	30

voltage noise and temperature distribution are space-dependent over the PDN area at certain resonance frequencies, the electric and thermal field profiles are intentionally captured.

The rest of this paper is organized as follows. In Section II, the typical structure of the on-chip PDN grid is introduced, and the temperature-dependent material parameters are summarized. In Section III, the development process of the frequency-domain electrothermal co-simulation solver is presented. In Section IV, the accuracy of the co-simulation solver is verified, and the impacts of excitation condition, dielectric loss tangent, and TSV location on the electrothermal characteristics of 3-D PDN are discussed. Some conclusions are drawn in Section V.

II. Model Description

A. On-Chip PDN Structure

A typical structure of the on-chip PDN grid with two global-level metal layers is shown in Fig. 1, where the power and ground lines are illustrated by the red and blue lines, respectively. In each metal layer, six power and five ground lines are arranged alternately over the chip area and are orthogonal to the lines of the other metal layer. Cubic metal contacts are put at the P/P (G/G) sites to connect the power (ground) lines of two metal layers together. The on-chip PDN is embedded in a $2.2 \times 2.2 \times 0.12\text{-mm}^3$ interlayer dielectric (ILD) layer, and its size is 2.03×2.03 mm^2. Other geometrical parameters of the power/ground lines and the contacts are listed in Table I.

The voltage of the on-chip global-level power grid is supplied by the on-board voltage regulator module; then, it goes through vias and lower level power grids to reach the transistors. The power and ground nets are physically separated, so ideally, no current passes through the PDN structure, and a constant supply voltage is provided to all power requiring devices. However, during the transistor's switching process, transient current containing high-frequency components passes through the PDN and causes significant voltage noise. Moreover, as aforementioned, the thermal integrity becomes a critical problem in 3-D ICs due to the long current path in PDNs.

TABLE II
MATERIAL PROPERTIES

Material	Real relative permittivity ε_r'	Resistivity ρ (Ω·m)	Loss tangent $\tan\delta_d$	Thermal conductivity k (W/m-K)
Cu	1	(1)	0	(2)
Si	11.9	(4)	0	(3)
ILD	2.2 [22]	/	0-0.1 [22]	0.12 [23]
Air	1	/	0	0.026

B. Material Properties

The electrical and thermal parameters of the materials involved in this paper are summarized in Table II. The temperature-dependent resistivity of Cu is calculated by [14]

$$\rho_{\text{Cu}} = \rho_0[1 + \alpha(T - T_0)] \tag{1}$$

where $\rho_0 = 1.7 \times 10^{-8}\ \Omega \cdot \text{m}$ is the bulk resistivity at room temperature $T_0 = 300$ K, and $\alpha = 3.9 \times 10^{-3}\ \text{K}^{-1}$ is the temperature coefficient of resistivity. The thermal conductivities of Cu and Si are given as [17]

$$k_{\text{Cu}} = -6.81 \times 10^{-2}\ T + 420.33\ (200\ \text{K} \le T \le 1200\ \text{K}) \tag{2}$$

$$k_{\text{Si}} = 2.475 \times 10^{5}\ T^{-1.3}\ (273\ \text{K} \le T \le 1000\ \text{K}). \tag{3}$$

The Si substrate is assumed as p-type Si, and its hole-doping concentration N_a is 1.25×10^{15} cm^{-3} [20]. The Si resistivity can be calculated by [21]

$$\rho_{\text{Si}} = \frac{1}{e\mu_p N_a} \tag{4}$$

where $e = 1.6 \times 10^{-19}$ C is the electron charge. $\mu_p \propto T^{-2.2}$ (300 K $\le T \le$ 500 K) is the hole mobility, and it equals 480 cm^2/V·s at room temperature. It is evident that the temperature has a negative influence on the electrical and thermal conductivities of Cu and Si.

With both conductor and dielectric losses considered, the permittivity of a material can be written as a general form, that is

$$\varepsilon = \varepsilon_0\left(\varepsilon_r' - j\varepsilon_r'' - j\frac{\sigma}{\omega\varepsilon_0}\right) = \varepsilon_0\varepsilon_r'(1 - j\tan\delta_d - j\tan\delta_c) \tag{5}$$

where $\tan\delta_d = \varepsilon_r''/\varepsilon_r'$ is the dielectric loss tangent, and $\tan\delta_c = \sigma/(\omega\varepsilon_0\varepsilon_r')$ is the conductor loss tangent. ε_0 is the permittivity in vacuum, ε_r' and ε_r'' are the real and imaginary parts of the relative permittivity, ω is the angular frequency, and σ is the conductivity. For a conductor, $\tan\delta_c$ is much larger than $\tan\delta_d$, while for a dielectric, $\tan\delta_d$ is the dominant term.

As indicated in [22], organosilicate glass (SiOCH) is recognized as a promising low-k porous dielectric for a 45-nm technology node and beyond. It is adopted as the ILD material

in our simulation. The dielectric loss of the SiOCH is mainly caused by the moisture absorption during the process steps, and the extracted dielectric loss tangent $\tan\delta_d$ can reach as high as 0.1. Its thermal conductivity is calculated to be 0.12 according to the porosity-weighted simple medium model [23], [24].

III. FEM Implementation

The basic principles and development process of the frequency-domain electrothermal co-simulation solver using FEM are presented in this section. The mutual interaction of electrical and thermal fields is considered through a cyclic solution process.

A. Electrical Boundary Value Problem

The full-wave electromagnetic analysis solves the following vector wave equation [14]:

$$\nabla \times \left(\frac{1}{\mu}\nabla\times\vec{E}\right) - \omega^2\varepsilon\vec{E} = -j\omega\vec{J} \tag{6}$$

where μ is the permeability, ε is the complex dielectric constant given in (5), $\vec{J}$ is the added current source, and $\vec{E}$ is the electric field vector to be solved. To truncate the open space into a finite computation region, the following first-order absorbing boundary condition is adopted:

$$\frac{1}{\mu}\vec{n}\times(\nabla\times\vec{E}) + j\omega\sqrt{\frac{\varepsilon}{\mu}}\vec{n}\times(\vec{n}\times\vec{E}) = 0 \tag{7}$$

where $\vec{n}$ is an outward-pointing unit vector.

Here, the volume is meshed into numerous small tetrahedron elements, and the electric field in each element can be expressed as

$$\vec{E}^e = \mathbf{x}^{e^T}\vec{\mathbf{N}}^e \tag{8}$$

where $\vec{\mathbf{N}}^e$ and $\mathbf{x}^e$ are the arrays of vector basis functions and their associated electric field unknowns, respectively. By applying the Ritz method and assembling all elemental matrices, the solution of the boundary value problem can be obtained by solving a set of linear equations as

$$(\mathbf{K}_0 - \omega\mathbf{K}_1 - \omega^2\mathbf{K}_2)\mathbf{x} = \mathbf{K}\mathbf{x} = \omega\mathbf{b} \tag{9}$$

where $\mathbf{K}_0$ and $\mathbf{K}_2$ are the basic terms, $\mathbf{K}_1$ is a term related to the absorbing boundary condition in (7), and they are all sparse symmetric matrices. $\mathbf{b}$ is a current-related vector, and $\mathbf{x}$ is the only unknown term to be solved. The related elemental matrices are given as [15]

$$\mathbf{K}_0^e = \frac{1}{\mu^e}\int_{V^e}(\nabla\times\vec{N}^e)\cdot(\nabla\times\vec{N}^e)^T dV \tag{10}$$

$$\mathbf{K}_1^e = -j\sqrt{\frac{\varepsilon}{\mu}}\int_{S^e}(\vec{n}\times\vec{\mathbf{N}}^e)\cdot(\vec{n}\times\vec{\mathbf{N}}^e)^T dS \tag{11}$$

$$\mathbf{K}_2^e = \varepsilon^e\int_{V^e}\vec{\mathbf{N}}^e\cdot\vec{\mathbf{N}}^{e^T} dV. \tag{12}$$

A line current I is added on an edge k as

$$b_k = -j\int_{\text{edge } k}\vec{\mathbf{N}}_k\cdot I\cdot d\vec{l}_I \tag{13}$$

where k is the global edge number. After adding the current source on port j, the value of $\vec{E}$ in the whole structure can be obtained, and then the voltage on port i (V_i) can be calculated by adding up the corresponding electric field components. Finally, the PDN impedance parameters can be calculated by

$$Z_{ij} = \left.\frac{V_i}{I_j}\right|_{I_k=0,\ k\neq j}. \tag{14}$$

In the FEM implementation, the solving of (9) consumes more computer resources in the whole calculation process. As we know, the preconditioned biconjugate gradient (PBCG) method has high efficiency in solving a kind of linear system of equations whose $\mathbf{K}$ matrix is sparse, complex, symmetric, and positive definite. Therefore, the PBCG method is employed here to speed up the computational efficiency. Moreover, the element-by-element (EBE) approximate factorization method is used in each iterative process of PBCG, i.e., the matrix–vector multiplier is conducted at element level in parallel [18].

B. Thermal Boundary Value Problem

The thermal boundary value analysis is governed by the heat conduction equation

$$-\nabla\cdot(k\nabla T) = f_0 \tag{15}$$

with the Dirichlet boundary condition

$$T = T_d \tag{16}$$

and the air convection boundary condition

$$\vec{n}\cdot(k\nabla T) = -h(T - T_a) \tag{17}$$

where T is the temperature, k is the thermal conductivity, f_0 is the input power density (W/m^3), T_d is the temperature on Dirichlet boundary, h is the heat convection coefficient, and T_a is the ambient temperature.

The Joule heat associated with the power from conductor loss and dielectric loss is taken as the heat source f_0 as

$$f_0 = \frac{1}{2}\left(\sigma + \omega\varepsilon_0\varepsilon_r''\right)|\vec{E}|^2 \tag{18}$$

where $\vec{E}$ is the electric field intensity obtained by solving the electric boundary value problem in Section III-A. With the input f_0, the temperature can be obtained by solving (15) using FEM. The temperature rise will in turn change the values of temperature-dependent material parameters, such as the electrical and thermal conductivities, as listed in Table II. Then, based on the updated material parameters, new values of the electric field and temperature can be obtained by successively solving the electrical and thermal boundary value problems one more time. Repeat the coupling process until the difference between two successive results becomes smaller than a given threshold value. The result of the last iteration is regarded as the final result after considering the mutual interactions of electric and thermal fields. In this electrothermal iteration process, the calculated result of the previous iteration can be used as the original value of the PBCG in the next iteration, which can greatly reduce the PBCG solution time of the latter iteration.

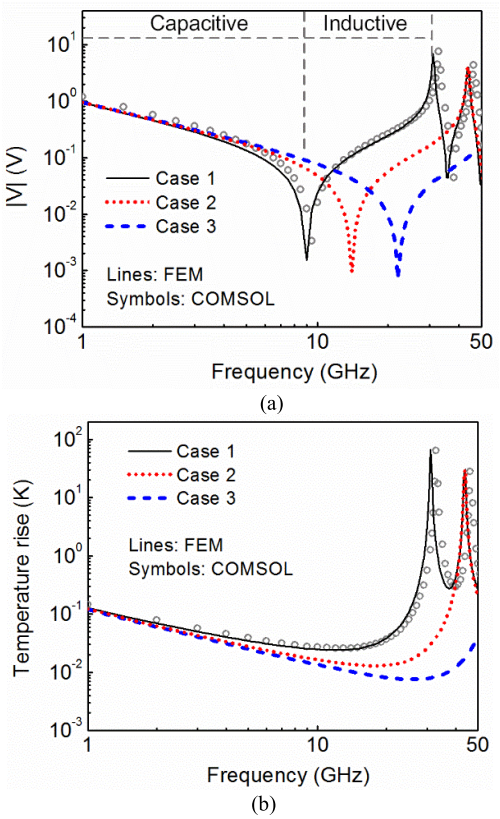

Fig. 2. (a) Amplitude of the on-chip PDN voltage detected at port A for different cases of excitation. (b) Maximum temperature rise of the on-chip PDN.

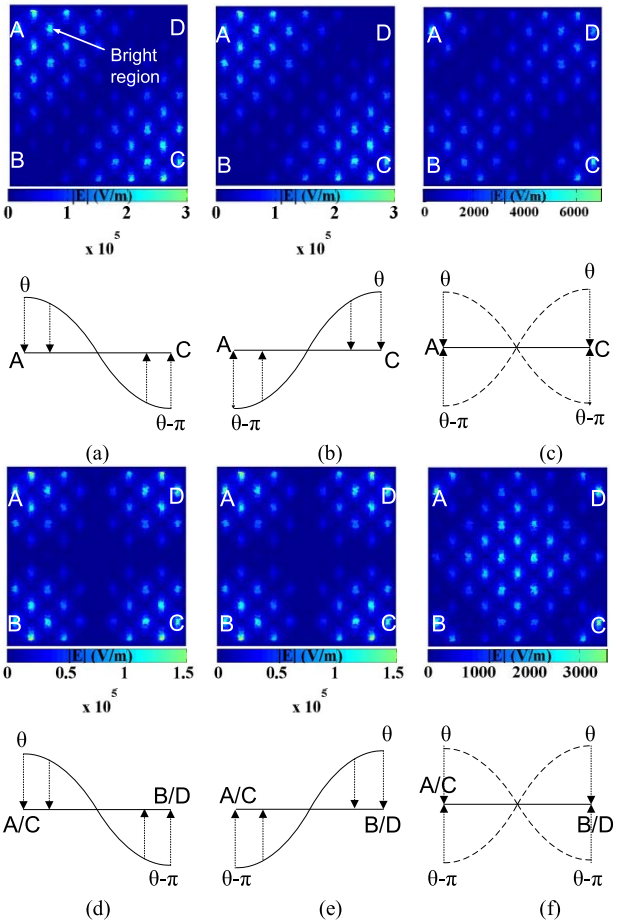

Fig. 3. Electric field profiles in *xy* plane through the contact layer in Fig. 1 at the resonant frequency of 32 GHz for (a) 5-mA input at port A, (b) 5-mA input at port C, and (c) 2.5-mA input at ports A and C, and at 45 GHz for (d) 5-mA input at port A or C, (e) 5-mA input at port B or D, and (f) 1.25-mA input at ports A–D.

IV. Results and Discussion

In this section, the FEM-based electrothermal co-simulation solver is used to investigate the electrothermal characteristics of 3-D PDNs. The influence of the excitation condition and dielectric loss tangent is analyzed for the on-chip power grid, and the influence of TSV location is discussed for a TSV-based two-chip PDN structure.

A. Influence of Excitation Condition

First, the on-chip power grid shown in Fig. 1 is simulated for different excitation conditions. The temperature-dependent material parameters in Table II are utilized in the electrothermal co-simulation process. The loss tangent of the surrounded ILD is set to be 0.01. In the FEM implementation, the whole structure is surrounded by an air box. In an electrical simulation, an absorbing boundary condition is applied on the outside wall of the air box to avoid reflections in the computation domain. In the thermal simulation, a convection boundary condition is used with a heat convection coefficient h of 10 W/m$^2 \cdot$ K and an ambient temperature of 300 K.

Three cases are studied by inputting current at different ports. In case 1, a 5-mA line current is inputted at port A, as shown in Fig. 1. In case 2, line currents of 2.5 mA are inputted simultaneously at ports A and C, which are in central symmetry on the chip. In case 3, line currents of 1.25 mA are inputted simultaneously at ports A–D. The voltage curves probed at port A for these three cases as functions of frequency are plotted in Fig. 2(a). The maximum temperature rise in Fig. 2(b) is calculated as the maximum temperature of the whole structure minus the ambient temperature. The voltage and temperature results for case 1 obtained from the commercial simulator COMSOL Multiphysics are also plotted in Fig. 2 to verify the accuracy of our electrothermal co-simulation solver, and the results agree well with each other.

According to (14), self-impedance Z_{11} is defined as the voltage-to-current ratio at the same port. In case 1, as I is a constant, the induced voltage curve in Fig. 2(a), therefore, has a similar shape with that of $|Z_{11}|$. From the voltage curve of case 1, the on-chip PDN behaves like a capacitive element at frequencies below several gigahertz. After the first valley value at about 9 GHz, it starts to behave like an inductive element, and the impedance increases with the frequency up to the first resonance peak at 32 GHz. Then, a second resonance peak occurs at 45 GHz.

The peak at 32 GHz is suppressed in case 2, and both peaks are suppressed in case 3 as shown in Fig. 2. The electric field's amplitude and phase information in Fig. 3 are used to explain the suppressed resonances according to the superposition principle of the electric field. Fig. 3(a) shows the distribution of the electric field at 32 GHz with a 5-mA

current inputted at port A, and Fig. 3(b) shows the profile when putting the current at port C. They both have a half-wavelength cosine distribution along the diagonal (A–C) direction but are in antiphase (i.e., have a phase difference of π). In Fig. 3(c), ports A and C are excited; simultaneously, the encounter of these two antiphase waves results in a much lowered electric field because of the destructive interference. Numerically, when port A is excited alone in Fig. 3(a), the induced plural voltage at port A is $(6.3+3j)$ V, with an amplitude of 7 V and a phase of 0.14π. When port C is excited alone in Fig. 3(b), the voltage at port A is probed to be $(-6.3-2.6j)$ V, with an amplitude of 6.8 V and a phase of -0.88π. In Fig. 3(c), adding up these two voltages and then divided by two, the voltage at port A is calculated to be $0.2j$ V with an amplitude of 0.2 V and a phase of 0.5π. In this way, with a phase difference of 1.02π, when ports A and C are excited together, the amplitude of the electric field is lowered by more than 30 dB (from 7 and 6.8 to 0.2 V), which reasonably explains the suppression of resonance at 32 GHz for case 2. In the same way, when a 5-mA current is inputted at port A/C at 45 GHz, the induced electric field has similar amplitude but a phase difference of π with that of putting current at B/D as shown in Fig. 3(d) and (e). Both figures have a half-wavelength cosine-type profile along each edge of the PDN square. Again, because of the superposition of these antiphase electric fields, the field value in Fig. 3(f) when four ports are excited at the same time is largely lowered, and thus, the resonance at 45 GHz is suppressed for case 3. In general, if two points in antiphase places of the power grid, that is, having a distance of odd times of half-wavelength, are excited simultaneously, a much lowered voltage noise can be achieved because of the superposition of electric field. Note that the calculated voltage from the superposition principle strictly equals the value directly extracted from the co-simulation solver, further verifying the accuracy of our FEM programs. As we know, the electric field intensity between two conductors with certain voltage difference is inversely proportional to their distance. At the P/G overlap sites in Fig. 1, the power and ground nets are closest to each other, leading to the locally strengthened electric field as shown by the bright regions in Fig. 3.

The maximum temperature rise of the on-chip PDN is plotted in Fig. 2(b). The maximum temperature rise can reach up to several tens of degrees, and the peak values occur at the same frequencies as the resonance peaks in Fig. 2(a). This is because a peak PDN impedance will result in a peak power dissipation, thereby leading to a peak temperature rise from the self-heating of the PDN structure. It is evident that depressing the resonances can not only lower the PDN impedance but also subdue the temperature rise. Moreover, it can be seen in Fig. 2(b) that there is no valley value in the temperature rise curves, although the voltage curves have valley values at 9, 14, and 22 GHz. This can be explained in two aspects. First, the voltage is captured at a specific point, while the maximum temperature rise is for the whole structure. Second, the voltage is decided by the electric field in the dielectric between the power and ground lines, while the temperature is determined by the loss power in both conductor and dielectric, which will be discussed in Section IV-B.

TABLE III
COMPARISON OF SIMULATION TIME BETWEEN THE PROPOSED SOLVER AND COMMERCIAL SOFTWARE COMSOL MULTIPHYSICS FOR STUDYING ON-CHIP PDNS WITH DIFFERENT METAL LAYERS

Number of metal layers	Number of mesh elements ($\times 10^4$)	Simulation time (s)	
		Co-simulation solver	COMSOL Multiphysics
2	6.0	111	224
3	8.7	200	327
4	10.9	322	500
5	11.4	381	518

In practical applications, the on-chip power grid may contain more than two metal layers. Table III compares the simulation time of a single frequency point between the proposed solver and COMSOL Multiphysics for studying on-chip PDNs with different metal layers. The simulations are carried out on a personal computer (Core-4 CPU at 3.3 GHz, 4-GB RAM), and the same mesh is employed. It is evident that the increase in metal layers requires more mesh elements, thereby consuming longer simulation time. Thanks to the PBCG-EBE method, the proposed co-simulation solver consumes less CPU time than does COMSOL Multiphysics.

B. Influence of Dielectric Loss Tangent

Based on the structure shown in Fig. 1, the impact of the dielectric loss tangent on the electrothermal characteristics of the on-chip PDN is discussed here. A line current I of 5 mA is inputted at port A. The self-heating power from the conductor (dielectric) loss part of the whole PDN structure given in Fig. 4(a) is captured by adding up the conductor (dielectric) loss power of each small tetrahedron element meshing the structure. The corresponding maximum temperature rise caused by both the conductor and dielectric losses in Fig. 4(a) is plotted in Fig. 4(b).

As shown in Fig. 2, the peak values appear at 32 and 45 GHz for both the power and maximum temperature rise in Fig. 4, which are caused by the resonance peaks. From Fig. 4(a), when $\tan\delta_d$ increases from 0.01 to 0.1, the power from dielectric loss is apparently improved, while that from conductor loss remains almost unchanged except at the resonance frequencies. On resonance frequencies, however, the power and maximum temperature rise in the case of $\tan\delta_d = 0.1$ are smaller than those in the cases of $\tan\delta_d = 0$ and $\tan\delta_d = 0.01$ because the severe dielectric loss largely lowers the intensity of resonances.

When $\tan\delta_d = 0.01$, the power from dielectric loss is higher than that of conductor loss in the frequencies up to 10 GHz, and they become comparable to each other in high frequencies. When $\tan\delta_d$ increases to 0.1, the loss in dielectric becomes dominant over the whole frequency range, as shown in Fig. 4(a). As shown in Fig. 4(b), the maximum temperature increases significantly with the increasing dielectric loss tangent, which means that the dielectric loss cannot be simply neglected in the PDN simulations.

Fig. 5(a) and (b) shows the electric field profiles through the contact layer and the metal layer at 32 GHz for the on-chip PDN with $\tan\delta_d = 0.01$. The corresponding temperature distribution is plotted in Fig. 5(c). In the contact layer,

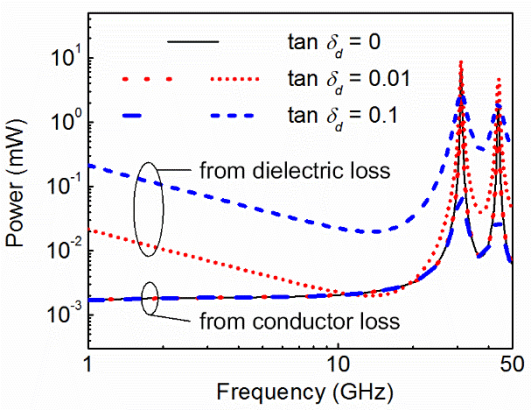

Fig. 4. (a) Power from conductor or dielectric loss. (b) PDN's maximum temperature rise as functions of frequency for a different dielectric loss tangent.

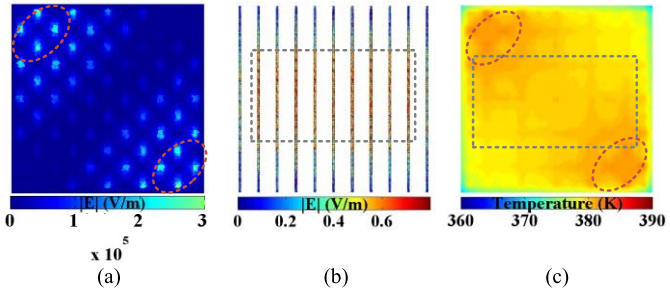

Fig. 5. Electric field profiles in *xy* plane through (a) contact layer and (b) upper metal layer at 32 GHz. (c) Corresponding temperature profile through ILD.

the strengthened electric field at the P/G overlap sites causes severe loss in the low-*k* dielectric and leads to the apparent temperature rise at the upper-left and lower-right corners of Fig. 5(c) (marked by circles). In the metal layer, the electric field is large in the middle region of the chip and causes the temperature rise in the middle area marked by the rectangle. It can be seen in Fig. 5(c) that the regions near the orthogonal metal lines show higher temperature. This is because metal lines can effectively spread heat from hot spaces to cool regions.

C. TSV Location

In a two-chip stack in 3-D integration, TSVs are used to connect the power grid of the two stacking chips together as

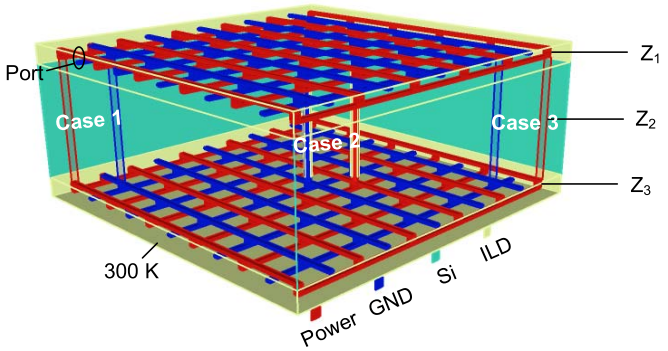

Fig. 6. Schematic of a TSV-based two-chip PDN structure. Cases 1–3 represent different locations of the TSV pair. The plane $z = Z_1$ goes through the middle of the upper chip, plane $z = Z_2$ through the middle of TSV, and plane $z = Z_3$ through the middle of the lower chip.

shown in Fig. 6. This two-chip PDN structure is composed of two on-chip power grids, each of which is the same with that of Fig. 1, and a pair of power and ground TSVs. The TSVs are surrounded with a 4-μm-thick dielectric layer for electrical isolation. The TSV diameter and height are 40 and 160 μm, respectively, and the height of the silicon substrate is 100 μm. Material parameters are taken from Table II, and the dielectric loss tangent of the ILD is set to be 0.01. The temperature of the bottom surface is set as 300 K. A line current I of 20 mA is inputted at the port shown in Fig. 6.

Here, the TSV pair is located at the upper-left corner, center, and lower-right corner, respectively, which are marked as cases 1–3, as shown in Fig. 6. The corresponding self-impedance and the maximum temperature rise of the PDN structure are shown in Fig. 7. Fig. 8 shows the temperature profiles of *xy* plane at different heights.

In the low-frequency region, it can be seen in Fig. 7(a) that the PDN impedance exhibits a capacitive behavior and is kept almost unchanged with the different TSV locations. Up to the inductive frequency region, the impedance increases significantly as the TSV pair moves away from the input port, as shown in Fig. 7(a). In the inductive range, the impedance is mainly determined by the inductance of the PDN loop at the signal routing, which contains both the on-chip PDN part and the TSV pair. When the TSV pair moves farther from the input port, the length of the signal routing becomes longer, and the inductance increases. The increased inductance also causes the decrease in the first impedance valley frequency, that is, from 6 to 5 and 4.3 GHz.

All three cases have an impedance peak at near 30 GHz, which is thought to be caused by the first on-chip resonance mode of the upper chip for three reasons: 1) the occurrence of the resonance is not influenced by the TSV location; 2) the resonance mode occurs almost at the same frequency as the first impedance peak of the single-chip PDN, which is at 32 GHz according to Fig. 2; and 3) the temperature profile of the upper chip under the resonance is shown in Fig. 8(a), and it has a similar pattern as that of the single-chip case in Fig. 5(c), that is, the heat is concentrated at the upper-left and lower-right corners. Unlike the single-chip PDN with the first resonance peak at 32 GHz, the existence of the TSV pair and the lower

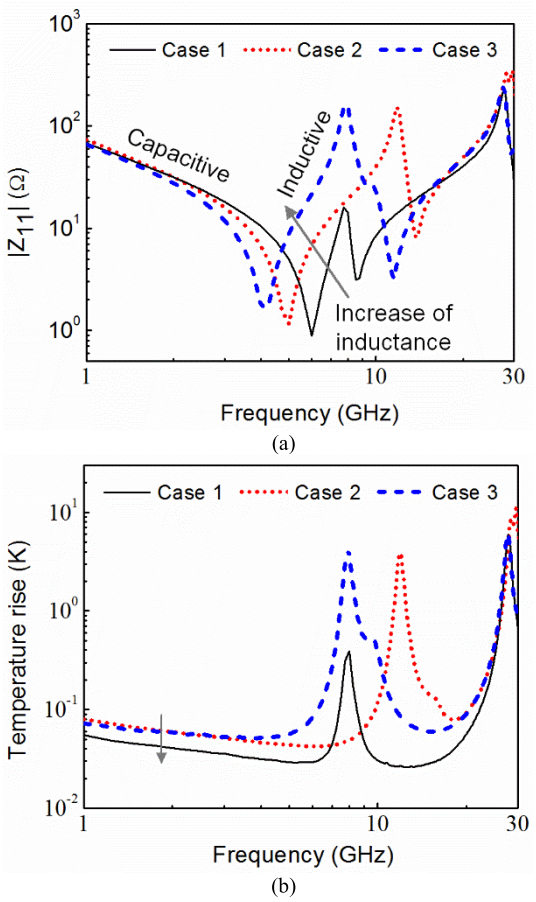

Fig. 7. (a) Z_{11} parameter and (b) maximum temperature rise of the two-chip PDN structure with different TSV locations.

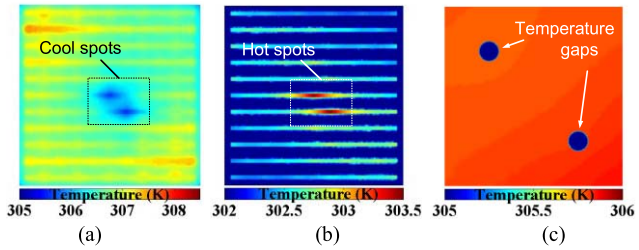

Fig. 8. Temperature profiles of plane (a) $z = Z_1$, (b) $z = Z_3$, and (c) enlarged TSV surrounding region at $z = Z_2$ for case 2 at 29.5 GHz.

chip causes additional chip-TSV resonance modes in the two-chip stack and leads to the additional impedance peaks at 7.8, 11.8, and 8 GHz for different TSV locations, as shown in Fig. 7. As the impedance value of the PDN structure is preferred to be low from dc to high frequency, compared to the single-chip case, the performance of the two-chip stack is exacerbated by these additional chip-TSV resonances.

As shown in Fig. 7(b), the maximum temperature rise is not apparent in the low-frequency region, and temperature peaks exist at the resonance peak frequencies. In the low-frequency region, the hot spot is located near the input port according to the simulation, so the TSV pair in case 1 can serve as an effective heat removal path, which is the reason why case 1 shows lower temperature rise than the others. The capability of TSVs as heat removal path can be clearly observed in Fig. 8 for case 2. The TSV pair helps to spread heat from the upper chip to the lower chip, causing the cool spots in the temperature profile of the upper chip in Fig. 8(a) and the hot spots in the temperature profile of the lower chip in Fig. 8(b). In Fig. 8(c), the surrounding area of the TSV pair in $z = Z_2$ plane is enlarged, where severe temperature gaps are observed in the thin dielectric layer between the TSV and the silicon substrate.

TABLE IV
COMPARISON OF SIMULATION TIME BETWEEN THE PROPOSED SOLVER AND COMMERCIAL SOFTWARE COMSOL MULTIPHYSICS FOR STUDYING TWO-CHIP PDNS WITH TSV PAIR AND TSV ARRAY

TSV	Number of mesh elements ($\times 10^5$)	Simulation time (s)	
		Co-simulation solver	COMSOL Multiphysics
TSV pair	1.0	512	731
TSV array	1.4	541	1011

Finally, the efficiency of the co-simulation solver in studying the TSV-based PDN structure is given in Table IV. The case of the TSV pair takes the data of case 2, i.e., putting a TSV pair at the center of the chip area. In the case of a TSV array, TSVs are located uniformly over the chip area. Therefore, 36 power TSVs and 25 ground TSVs are used in the simulation. It can be seen that the proposed co-simulation solver can save certain simulation time as compared to COMSOL Multiphysics.

V. CONCLUSION

In this paper, an efficient electrothermal co-simulation solver in the frequency domain is developed using FEM by solving the wave equation for the electromagnetic field and the heat conduction equation for the thermal field. This solver is used to simulate the electric and thermal problems in PDN structures in 3-D chip stack, containing an on-chip power delivery grid and TSVs. PDN impedance and the maximum temperature are calculated, and the related electric and thermal field profiles are obtained. Several conclusions can be made from the analysis to help to keep the electric and thermal integrity in 3-D integration. First, certain voltage peaks can be effectively suppressed when the PDN is excited simultaneously at several antiphase places because of the superposition of the electric field. Second, in the modeling of some low-*k* materials as SiOCH, the dielectric loss tangent is necessary to be taken into account. Third, compared to one-chip PDN, the impedance of a two-chip stack is exacerbated by the chip-TSV resonance modes.

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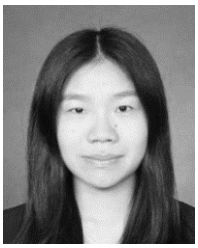

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