A New Compact Power Divider Based on Capacitor Central Loaded Coupled Microstrip Line

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***Abstract*— A new power divider is proposed with a compact size. In 50-Ω systems, impedance transformation is of great importance for power dividers. Coupled microstrip lines with capacitor loaded and two short-circuited ports are introduced to properly transform impedance and increase degrees of freedom in power divider designs. Image impedance and image transfer constant of coupled microstrip lines with capacitor loaded are derived. The main structural parameters of the power divider are calculated accordingly. A special design procedure is illustrated for the proposed power divider with the capacitor loaded, which is implemented on a printed circuit board. A good agreement between the simulated model and the fabricated sample is observed, which demonstrates the validity of the proposed circuit model and the design scenario.**

***Index Terms*— Coupled microstrip lines, image impedance, image transfer constant, power divider.**

I. Introduction

With the development of 3-D integration technologies, multifunction transceiver attracts much attention in intelligent transportation systems (ITSs) [1]–[4]. One of the main challenges in multifunction systems is integrating radar and communications RF front end, including antennas in a compact space [3]. The power divider is an important passive component to compose a complex RF front end in multifunction multiport networks. In the circuit design stage, size, output port interval, and phase of the ports in power dividers are all important factors to be concerned.

The output ports of the conventional two-way Wilkinson power divider [5] are close to each other with only one isolation resistor. The distance between the output ports of the conventional two-way Gysel power divider [6] is about half wavelength with a more complex isolation network with two resistors. Hence, it is necessary to design a power divider with a more flexible spatial distribution and a more compact isolation network.

Moreover, impedance transformation is essential for a power divider in 50-Ω systems. A section of $(2n + 1)$ 90°(n is an integer) transmission line, a section of coupled microstrip or stripline with two ports, short or open [7], and many other complex structures can be used to transform impedance to a specified value. To design a power divider with a coupled microstrip line for in-phase or out-phase power dividing [8], the value of image impedance is essential to be calculated. The value of image impedance of coupled microstrip line with two ports short-circuited to ground or open-circuited is limited by fabrication technologies. To overcome this problem, we apply a section of a coupled microstrip line with central loaded lumped components and two ports, short or open, to achieve appropriate impedance transformation. Microstrip line with lumped components loaded has been used to develop coupler [9], balun [10], hybrid ring [11], filter [12], and filtering power divider [13]. Shie *et al.* [9] presented an equivalent circuit of a single cell in periodically loaded coupled microstrip lines and derived the expression of Bloch impedance and propagation constant for even/odd mode. However, the image impedance for different port configurations, open or short, has not been discussed in [9]–[13]. The analysis method in [9] and [14] is more suitable for periodical structures. The relationship between characteristic impedance in [9] is just one special case. Therefore, another problem arises, "how to calculate the image impedance when coupled microstrip lines are loaded by lumped components?" The analysis presented in [7], using wave propagation theory to calculate image impedance, is very complicated for coupled microstrip line loaded with lumped components. To resolve the problem, we derive the formulation of the image impedance for newly proposed structures by matrix conversion.

In recent years, multifunction passive components, for example, filtering power dividers have been discussed in [15]–[19]. A power divider with low-order filtering performance is demonstrated in this article.

This article is organized as follows. Section II presents a method to calculate the image impedance and image constant of a symmetric four-port network with two ports, short or open. After formula deriving and then comparing with those in [7], a more reasonable method is verified to analyze coupled microstrip lines with lumped components loaded. For symmetric structures in the proposed power divider, even/odd mode method can be used to reduce the complexity of analysis. Section III discusses the main parameters of a power divider. The implementation and performance of the proposed power divider will be demonstrated in Section IV.

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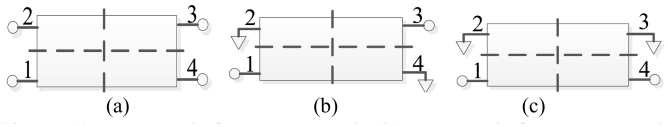

Fig. 1. (a) Symmetric four-port network. (b) Symmetric four-port network with the ports 2 and 4 short-circuited. (c) Symmetric four-port network with the ports 2 and 3 short-circuited.

II. Theoretical Analysis

A. Image Parameters of a Symmetric Four-Port Network

For a four-port symmetric, lossless, and reciprocal network shown in Fig. 1(a), its Y-matrix can be given as

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} Y_A & Y_B & Y_C & Y_D \\ Y_B & Y_A & Y_D & Y_C \\ Y_C & Y_D & Y_A & Y_B \\ Y_D & Y_C & Y_B & Y_A \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}. \tag{1}$$

The critical Y-parameters can be easily obtained with the input admittances Y_{ee}, Y_{eo}, Y_{oe}, and Y_{oo} of the equivalent even-/odd-mode quarter circuits in the symmetric four-port network by [14]

$$\begin{bmatrix} Y_A \\ Y_B \\ Y_C \\ Y_D \end{bmatrix} = \frac{1}{4} \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \\ 1 & -1 & 1 & -1 \end{bmatrix} \begin{bmatrix} Y_{ee} \\ Y_{eo} \\ Y_{oe} \\ Y_{oo} \end{bmatrix} \tag{2}$$

where the first and second subscripts of the input admittances correspond to the horizontal and vertical symmetric planes, respectively.

To analyze the coupled microstrip line with lumped components loaded, we derive the image parameters as [7]. If ports 2 and 4 are short circuited to the ground, as shown in Fig. 1(b), the two-port Y-matrix for the ports 1 and 3 is given by

$$\begin{bmatrix} I_1 \\ I_3 \end{bmatrix} = \begin{bmatrix} Y_A & Y_C \\ Y_C & Y_A \end{bmatrix} \begin{bmatrix} V_1 \\ V_3 \end{bmatrix}. \tag{3}$$

According to the relationship between Y-matrix and ABCD-matrix, the image impedance and image transfer constant can be derived by [7], [14]

$$Z_{I1}^2 = 1/\left(Y_A^2 - Y_C^2\right) \tag{4a}$$

$$\cos\varphi_1 = -Y_A/Y_C. \tag{4b}$$

Substituting (2) into (4), the image parameters of the two-port network shown in Fig. 1(b) can be calculated by

$$Z_{I1}^2 = \frac{4}{(Y_{ee}+Y_{oo})(Y_{eo}+Y_{oe})} \tag{5a}$$

$$\cos\varphi_1 = -\frac{Y_{ee}+Y_{eo}+Y_{oe}+Y_{oo}}{Y_{ee}-Y_{eo}-Y_{oe}+Y_{oo}}. \tag{5b}$$

If port 2 and 3 are short circuited to the ground, as shown in Fig. 1(c), the two-port Y-matrix for ports 1 and 4 is given by

$$\begin{bmatrix} I_1 \\ I_4 \end{bmatrix} = \begin{bmatrix} Y_A & Y_D \\ Y_D & Y_A \end{bmatrix} \begin{bmatrix} V_1 \\ V_4 \end{bmatrix}. \tag{6}$$

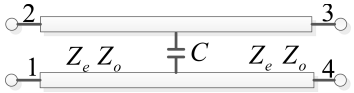

Fig. 2. Coupled microstrip line centrally loaded with a capacitor.

Similar to the above-mentioned derivation, the image impedance and image transfer constant of the two-port network are given by

$$Z_{I2}^2 = \frac{4}{(Y_{ee}+Y_{oe})(Y_{eo}+Y_{oo})} \tag{7a}$$

$$\cos\varphi_2 = -\frac{Y_{ee}+Y_{eo}+Y_{oe}+Y_{oo}}{Y_{ee}-Y_{eo}+Y_{oe}-Y_{oo}}. \tag{7b}$$

B. Coupled Microstrip Line Central Loaded With Lumped Capacitor

As shown in Fig. 2, a coupled microstrip line is loaded with a capacitor at its center. Then, the input admittances of the eigenmode quarter circuits are given by

$$\begin{cases} Y_{ee} = j\dfrac{1}{Z_e}\tan\theta \\ Y_{eo} = -j\dfrac{1}{Z_e}\cot\theta \\ Y_{oe} = j\dfrac{1}{Z_o}\dfrac{\omega C Z_o + \tan\theta}{1-\omega C Z_o\tan\theta} \\ Y_{oo} = -j\dfrac{1}{Z_o}\cot\theta. \end{cases} \tag{8}$$

Let $\tan\theta = t$ and substitute (8) into (5) and (7), the following equations for coupled microstrip lines can be derived:

$$Z_{I1}^2 = \frac{4Z_e^2Z_o^2t^2(1-\omega C Z_o t)}{\left[Z_e t^2 - Z_o + \omega C Z_o t(Z_e+Z_o)\right]\left(Z_e - Z_o t^2\right)} \tag{9a}$$

$$\cos\varphi_1 = \frac{\left(1-t^2\right)\left(Z_e+Z_o-\omega C Z_o^2 t\right) - 2\omega C Z_e Z_o t}{\left(1+t^2\right)\left(Z_o - Z_e - \omega C Z_o^2 t\right)} \tag{9b}$$

$$Z_{I2}^2 = \frac{4Z_e^2Z_o^2t(1-\omega C Z_o t)}{\left[(Z_o+Z_e)t + \omega C Z_o\left(Z_e - Z_o t^2\right)\right](Z_e+Z_o)} \tag{9c}$$

$$\cos\varphi_2 = \frac{\left(1-t^2\right)\left(Z_e+Z_o-\omega C Z_o^2 t\right) - 2\omega C Z_e Z_o t}{\left(1+t^2\right)\left(Z_o + Z_e - \omega C Z_o^2 t\right)}. \tag{9d}$$

If $C = 0$ in (9), the parameter equations for the coupled microstrip lines without capacitor loading can be obtained

$$Z_{I1} = \frac{2Z_eZ_o|\sin 2\theta|}{\sqrt{(Z_e+Z_o)^2\sin^2 2\theta - 4Z_eZ_o}} \tag{10a}$$

$$\cos\varphi_1 = \frac{Z_o+Z_e}{Z_o-Z_e}\cos 2\theta \tag{10b}$$

$$Z_{I2} = \frac{2Z_eZ_o}{Z_e+Z_o} \tag{10c}$$

$$\cos\varphi_2 = \cos 2\theta. \tag{10d}$$

It is found that (10) is the same as the equation in [7, Fig. 2(a) and (b)].

C. Power Divider Based on the Capacitor-Loaded Coupled Microstrip Line

A power divider is designed with the capacitor-loaded coupled microstrip line. Its schematic is shown in Fig. 3.

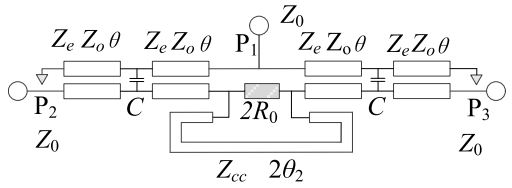

Fig. 3. Schematic of the proposed power divider.

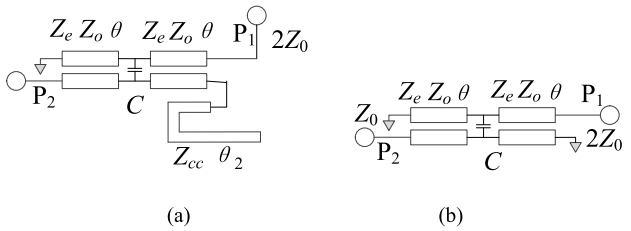

Fig. 4. (a) Even-mode half circuit of the proposed power divider. (b) Simplified even-mode equivalent circuit.

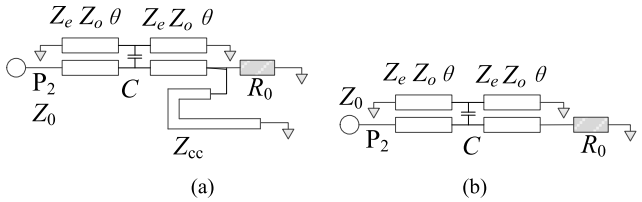

Fig. 5. (a) Odd-mode half circuit of the proposed power divider. (b) Simplified odd-mode equivalent circuit.

The power divider is different from the conventional Wilkinson or Gysel power dividers. Its isolation network is simpler than a Gysel power divider [6], whereas its output ports have a wider separation than a Wilkinson power divider [5]. Due to the symmetric structure, the even-/odd-mode analysis is applied.

The even-mode half circuit of the proposed power divider is shown in Fig. 4(a). If $\theta_2 = 90°$ at the design frequency f_d, the capacitor-loaded coupled microstrip line is further equivalent to the circuit shown in Fig. 4(b). In order to achieve good impedance matching, the capacitor-loaded coupled microstrip line should be equivalent to a quarter-wavelength transmission line, similar to a branch in a conventional two-way Wilkinson power divider. Then, the image parameters Z_{I1} and φ_1 should satisfy the following constraints at f_d [14]

$$Z_{I1}^2 = 2Z_0^2 \tag{11a}$$

$$\cos\varphi_1 = 0. \tag{11b}$$

The odd-mode half circuit of the proposed power divider is shown in Fig. 5(a), which can be further simplified and demonstrated by the circuit in Fig. 5(b) with $\theta_2 = 90°$ at f_d. To obtain good isolation, the image parameters Z_{I2} and φ_2 of the capacitor-loaded coupled microstrip line should satisfy the following constraints at f_d [14]

$$Z_{I2}^2 = Z_0 R_0 \tag{12a}$$

$$\cos\varphi_2 = 0. \tag{12b}$$

TABLE I

MAIN PARAMETERS OF THE POWER DIVIDER CALCULATED BY DIFFERENT Z_e, Z_o, AND RELATED m

Z_e	Z_o	θ	f_d	C_1	R_0	f_e	m
60	30	38.68	1.50	1.09	20.51	-	1
60	40	32.68	1.50	1.70	19.18	2.08	0.84
60	50	28.24	1.50	1.99	17.54	2.39	0.77
120	60	27.11	1.50	1.61	33.96	2.51	0.75
120	80	21.59	1.50	1.84	29.37	3.02	0.66
120	100	17.89	1.50	1.97	25.26	3.20	0.64

The unit of f is GHz; the unit of Z_e, Z_o, Z_{cc}, and R is Ohm; the unit of C_1 is pF, the unit of θ and θ_2 is degree; all the parameters are shown in Fig.3.

Substituting (9b) into (11b), it is derived as

$$\omega C Z_o = \frac{(1-t^2)(Z_e+Z_o)}{[2Z_e+(1-t^2)Z_o]t}. \tag{13}$$

Substituting (9a) into (11a), we have

$$\omega C Z_o = \frac{4Z_e^2Z_o^2t^2 - 2Z_0^2(Z_e - Z_o t^2)(Z_e t^2 - Z_o)}{2Z_0^2(Z_e+Z_o)(Z_e - Z_o t^2)t + 4Z_e^2Z_o^2t^3}. \tag{14}$$

Combining (13) and (14), the relationship among Z_o, Z_e, and $t = \tan\theta$ are deduced, and t is determined by a sixth-order polynomial. Solving the equation, the proper value of θ can be selected, which is a function of Z_o and Z_e. Then, C is determined by (13) or (14) with Z_o, Z_e, and θ. The value of R_0 can be obtained by (10c) and (12a).

III. DISCUSSION ON DESIGN PARAMETERS

A. Operating Bandwidth of the Proposed Power Divider

To verify our idea, two power divider prototypes are designed at the design frequency of 1.5 GHz, with ideal transmission lines and lumped components. The parameters of example 1 (E1) and example 2 (E2) are listed in Table I. The S-parameters can be calculated with the design parameters analytically, including Z_e, Z_o, θ, C, Z_{cc}, θ_2, and R_0. For example, the reflection coefficient of port 1 is given by

$$S_{11} = \frac{1 + (Y'_{22} - 2Y'_{11})Z_0 - 2(Y'_{11}Y'_{22} - Y'^2_{21})Z_0^2}{1 + (Y'_{22} + 2Y'_{11})Z_0 + 2(Y'_{11}Y'_{22} - Y'^2_{21})Z_0^2} \tag{15a}$$

$$Y'_{11} = Y_A - \frac{Y_D^2}{Y_A + Y_T} \tag{15b}$$

$$Y'_{22} = Y_A - \frac{Y_B^2}{Y_A + Y_T} \tag{15c}$$

$$Y'_{21} = Y_C - \frac{Y_B Y_D}{Y_A + Y_T} \tag{15d}$$

$$Y_T = j\frac{1}{Z_{cc}}\tan\theta_2. \tag{15e}$$

The calculated S-parameters are shown in Fig. 6. The operating band of such a power divider is identified that all the reflection coefficients S_{11}, S_{22}, and S_{33} and the isolation leakage S_{23} are better than -15 dB, whereas the transmission coefficients S_{12} and S_{13} are better than -3 ± 1 dB in the frequency band. The operating band is found to be 1.436–1.612 GHz for E1 and 1.411–1.612 GHz for E2. It is worth noting that the design frequency f_d is not precisely the central frequency in the operating band. It is caused by the different frequency

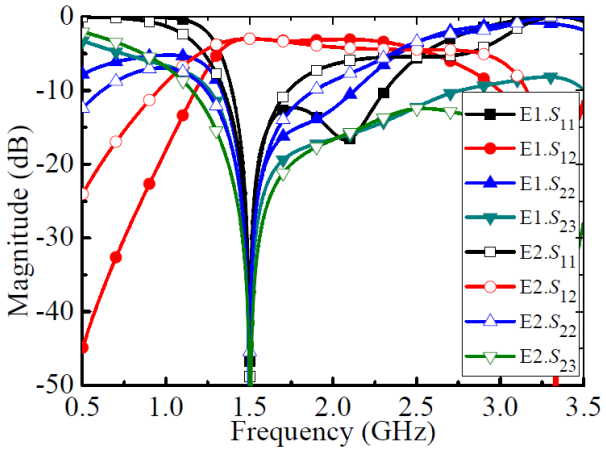

Fig. 6. Calculated S-parameters of the examples E1 and E2.

dependence of lumped capacitors and transmission lines. The fractional bandwidths (FBWs) of the two power dividers with ideal transmission lines and lumped components are both about 10%. Considering the performance degrading due to practical transmission lines and lumped components, it is necessary to increase the FBW in the design stage

B. Discussions on the Design Frequency

According to the previous discussions and observations from Fig. 6, the power divider with the design frequency f_d below the central frequency f_c will be a better choice. Based on Fig. 6, S_{11} is the main parameter to determine the FBW. As a result, the discussions on the design frequency f_d focuses on S_{11}. From the curves of S_{11} in Fig. 6, two local minima can be found. The first one is f_d, and the other one is denoted by f_e. Then, the central frequency f_c can be defined as

$$f_c = \frac{f_d + f_e}{2}. \tag{16}$$

The scaling factor m is defined as the ratio of the design frequency over the central frequency, given by

$$m = \frac{f_d}{f_c}. \tag{17}$$

The values of Z_e, Z_o, and m of different examples are listed in Table I. If Z_e is set to a fixed value, the electrical length θ and the scaling factor m decrease when Z_o increases, as shown in Table I. To get satisfactory results of reflection and isolation, Z_e and Z_o will be scaled by tuning m and other parameters as well shown in Table II.

The design procedure for the proposed power divider can be summarized as follows:

1) Identifying the initial central frequency f_c, according to (17) with the design frequency f_d. The initial scaling factor is named as m_1, with its value ranging from $0 < m_1 \leq 1$. If the curve of S_{11} only has one local minimum, m can be set to 1.
2) Providing initial values of Z_e and Z_o with achievable coupled microstrip lines.
3) Based on (13) and (14), calculating the parameters $\tan\theta$, and then choose an appropriate value of θ with the minimum electrical length from its solution space.
4) Calculating the value of capacitor C by (13) or (14). Based on (12a), calculating the value of mounted isolation resistor $2R_0$.
5) From the curves of S_{11} and (17), another scaling factor named m_2 can be calculated. Tuning Z_e and Z_o to enable $|m_1 - m_2|$ approaching 0, and then find out available values of capacitors and resistors that satisfy requirements of reflection and isolation bandwidth.

TABLE II
MAIN PARAMETERS OF THE POWER DIVIDER BEFORE AND AFTER SCALING

	E1		E2	
		Scaling factor		Scaling factor
f_c(GHz)	1.5	0.78	1.5	0.77
Z_e(Ohm)	60	1.09	120	0.97
Z_o(Ohm)	40	0.98	60	0.67
θ(deg)	32.68	1	27.11	1.35
C_1(pf)	1.7	0.89	1.61	0.7
R_0(Ohm)	19.18	1.32	33.96	1.07
Z_{cc}(Ohm)	50	0.9	50	0.93
θ_2(deg)	180	0.96	180	1.13

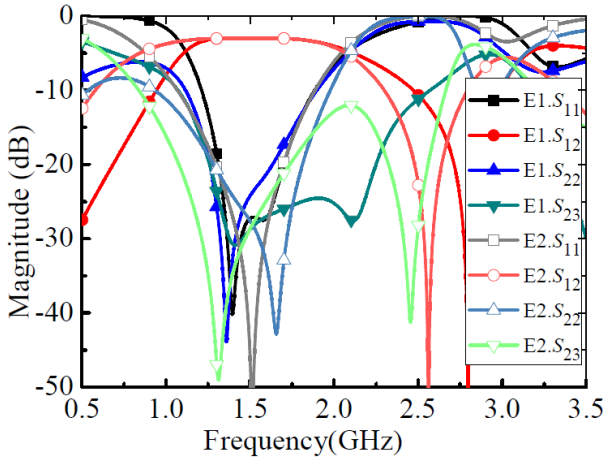

Fig. 7. Calculated scattering parameters S_{11}, S_{12}, S_{22}, and S_{23} of the circuit model with scaling factors shown in Table II.

We design two power dividers with central frequency around 1.5 GHz for E1 and E2, according to Table II. From Table II, the initial values of the scaling factor are about 0.78 and 0.77 for E1 and E2 to achieve larger bandwidth.

When the parameters are recalculated using the scaling factor, both power dividers have shown better reflection and isolation performance, as shown in Fig. 7.

In our design, Z_{cc} will affect power divider performance. When other parameters of E2 are determined by the scaling factor in Table II, it is found that the bandwidth will become smaller while the impedance Z_{cc} is increasing, as shown in Fig. 8. Considering the lower impedance microstrip line with much wider conductor width and larger size, Z_{cc} is selected to be equal to 50 Ω.

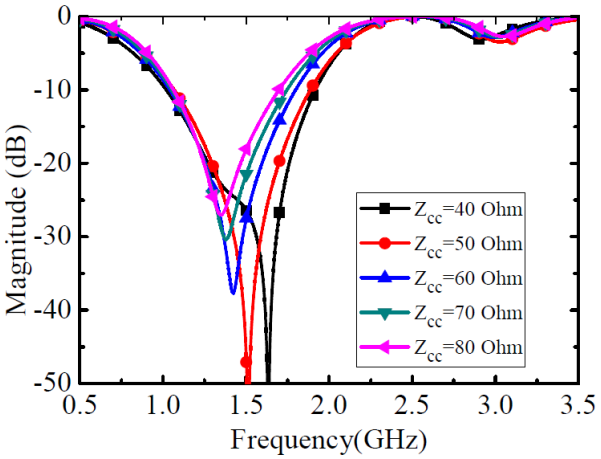

Fig. 8. Calculated scattering parameters S_{11} of the circuit model for E2 shown in Table II only for different Z_{cc}.

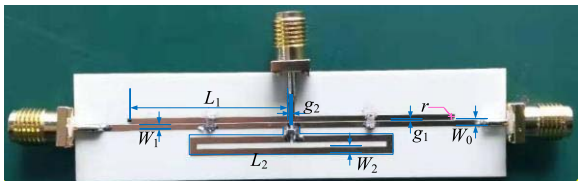

Fig. 9. Labeled photograph of the proposed out-phase power divider on microstrip.

IV. Results and Discussions

To verify the performance of the proposed method, a power divider with scaling parameters of E2 is fabricated on the printed circuit board of Rogers RO4350B with $\varepsilon_r = 3.66$ and $\tan\delta = 0.0031$. The thicknesses of the dielectric layer and metal layer are given by $h = 0.508$ mm and $t = 0.0035$ mm, respectively.

HFSS is used for full-wave simulation, and a vector analyzer of Agilent E5071 is used for measurement.

By simple tuning and optimizing, the dimensions are then given by $W_0 = 1.10$ mm; $W_1 = 0.93$ mm, $L_1 = 26.95$ mm; $W_2 = 1.14$ mm, $g_1 = 0.15$ mm, $g_2 = 0.40$ mm, $L_2 = 68.20$ mm, and $r = 0.25$ mm. The diameter of the metal cylindrical via is 0.5 mm. L_1 refers to the distance between the center of metal cylindrical via and the intersection of the T-junction. A surface-mounted resistor with specification 0603 is 47 Ohm, and a surface-mounted capacitor with specification 0805 is 1.3 pF. The total size is $0.46 \times 0.054\ \lambda_g^2$, and the photograph of the fabricated power divider is shown in Fig. 9. Simulated scattering parameters of the proposed power divider before optimization and after optimization are plotted in Fig. 10. From Fig. 10, it is evident that reflection and isolation performances are improved after optimization.

Simulated and measured scattering parameters of the proposed power divider are demonstrated in Fig. 11. The frequency range is 1.37–1.76 GHz for measured results with an FBW of about 24.9%, whereas S_{11}, S_{22}, S_{23}, and S_{33} are better than -15 dB, and S_{12} and S_{13} are better than -3 ± 1 dB.

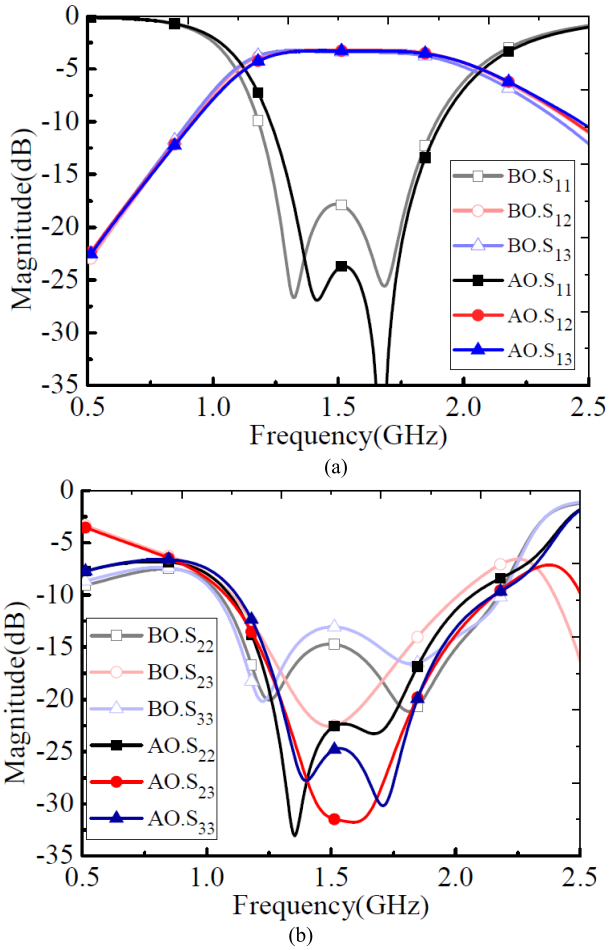

Fig. 10. Simulated scattering parameters of the proposed power divider. (a) S_{11}, S_{12}, and S_{13}. (b) S_{22}, S_{23}, and S_{33}. "BO." stands for simulated results before optimization, and "AO." stands for simulated results after optimization.

The frequency range under the same constraints of the aforementioned one is 1.3–1.82 GHz for simulated results with its FBW about 33.3%. The frequency range is 1.44–1.67 GHz for measured results with an FBW about 14.8%, in which S_{11}, S_{22}, S_{23}, and S_{33} are better than -20 dB, and S_{12} and S_{13} are better than -3 ± 1 dB. The frequency range is 1.34–1.76 GHz, with an FBW of about 27.1% for corresponding simulated results. The best insertion loss measured for S_{12} is -3.27 dB with an additional insertion loss of 0.27 dB at 1.44 GHz; that for S_{13} is -3.28 dB with an additional insertion loss of 0.28 dB at 1.43 GHz.

In 1.37–1.76 GHz, measured amplitude unbalance in Fig. 12 is below 0.2 dB; the measured phase unbalance is below 1.76°. In 1.3–1.82 GHz, simulated amplitude unbalance is below 0.1 dB, and simulated phase unbalance is below 0.75°.

The phase curves of S_{12} and S_{13} are plotted in Fig. 13. From Fig. 13, we find the measured phase curves show a steeper slope than simulated phase curves.

The discrepancy between the simulated and measured results may be caused by fabrication error, inhomogeneous material, and the error of capacitor or resistor values. This is because the discontinuity, the fabrication and inhomo-

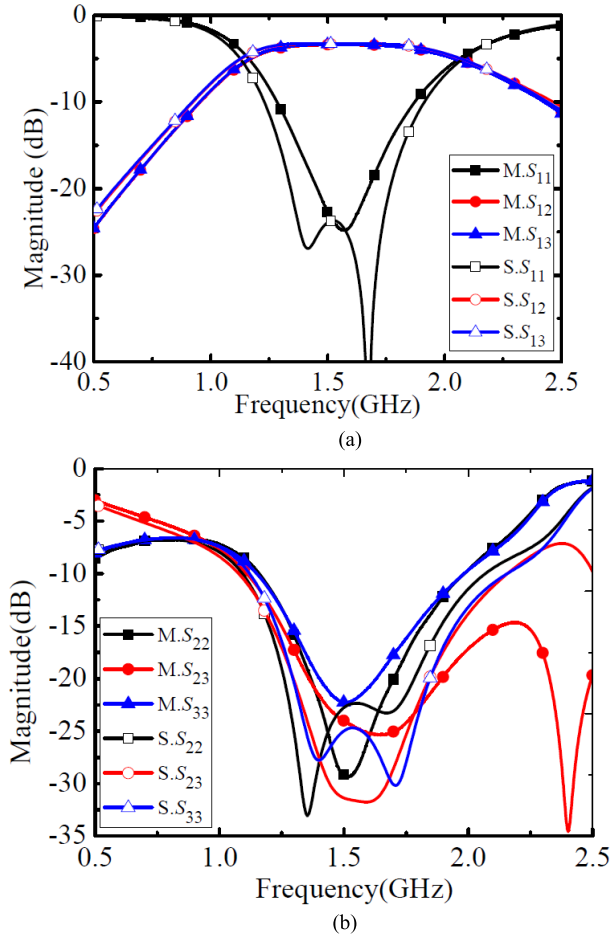

Fig. 11. Simulated and measured scattering parameters of the proposed power divider, (a) S_{11}, S_{12}, and S_{13} (b) S_{22}, S_{23}, and S_{33}. "S.:" stands for simulated results, and "M.:" stands for measured results. The same legend applies to the following figures.

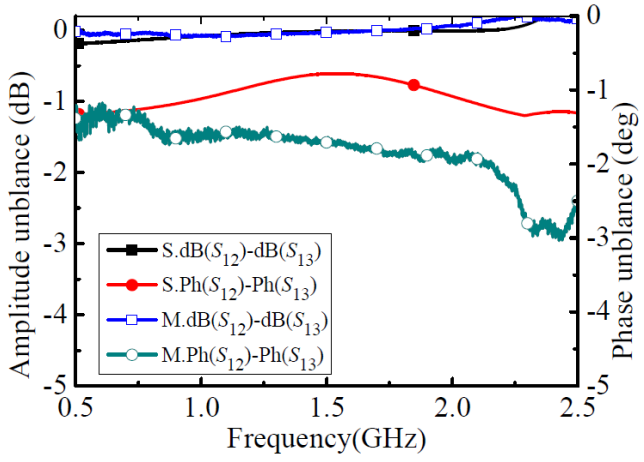

Fig. 12. Simulated and measured amplitude and phase unbalance of the proposed power divider. "Ph" refers to phases of S_{12} and S_{13} with the unit of degree, and "dB" refers to amplitudes of S_{12} and S_{13}.

geneous material, and the capacitor or resistor error have not been completely taken into account in simulation and calculation.

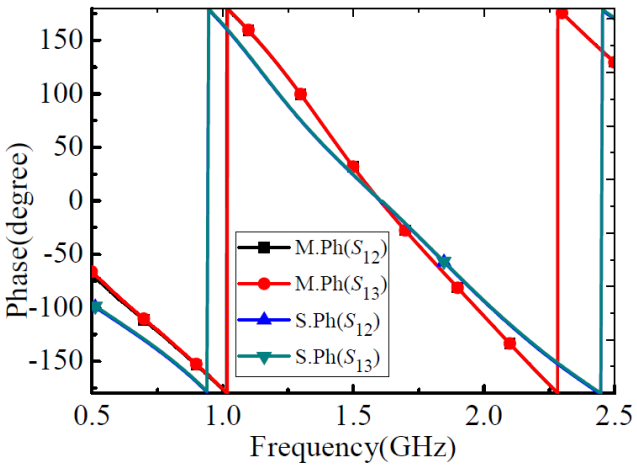

Fig. 13. Simulated and measured phases of S_{12} and S_{13} with the unit of degree.

TABLE III
COMPARISONS BETWEEN THE PROPOSED AND THE REFERENCES

Ref.	$\lambda_g \times \lambda_g$	f_0(GHz)	IL.(dB)	FBW15	AU.	PU.
[20.E1]	0.4×0.16	1.5	0.5	80.0%	<0.3	<3
[21.E1]	0.3×0.15	2	0.65	65%	-	-
[22.E1]	0.13×0.19	1.93	0.59	<10%	<0.19	<3.5
[23]	0.021	0.92	0.99	7%	-	-
[24]	<0.1×0.08	0.5	0.4	68%	-	-
[25]	0.13×0.19	1.4	1.3	15%	-	-
[26.E1]	0.3×0.17	3.5	0.9	<10%	-	-
[27.E1]	0.5×0.1	2	0.6	22%	-	-
this work	0.46×0.05	1.5	0.27	26.8%	<0.2	<1.76

"E1." refers to the first example in related reference. "IL." refers to the insertion loss; "FBW15" refers to -15dB fraction bandwidth for all reflection loss and isolation; "AU." refers to amplitude unbalance with the unit of dB; "PU." refers to phase unbalance with the unit of degree.

The comparison between the fabricated divider and other dividers in the literature is summarized in Table III. From Table III, the proposed design method of power divider can provide more degrees of freedom with compact size.

Next, we will discuss the degrees of designing freedom. Z_e and Z_o and electrical length θ have more degrees of freedom than a resistor and capacitor. Z_e, Z_o, and θ can be tuned to satisfy isolation and reflection performance, based on the capacitors and resistors available. Capacitors and θ can be determined by Z_e and Z_o at different designing frequency. Z_e and Z_o are restricted by the sizes of the coupled line. Therefore, the proposed power divider can be designed by finite capacitors and resistors at any frequency, where the fabrication process permits by tuning the sizes of a coupled line.

V. CONCLUSION

A new power divider is proposed to provide more degrees of freedom in the design stage. The image impedance of the capacitor loaded coupled microstrip line with ports, short or open, is derived. Then, even/odd mode analysis is used

for the symmetric structure of proposed power divider. Due to the asymmetry of the capacitance, the design procedure for the proposed power divider is different from conventional methods. Based on the proposed design procedure, we have designed a power divider with equal power ratio. The power divider is fabricated on Rogers RO4350. The performance is demonstrated by the simulated and measured scattering parameters.

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