Dielectric Resonators With High Q-Factor for Tunable Low Phase Noise Oscillators

Liang Zhou, *Member, IEEE*, Wen-Yan Yin, *Fellow, IEEE,* Jiang Wang, Lin-Sheng Wu, *Member, IEEE*

***Abstract*— This paper demonstrates the realization of tunable microwave low phase noise oscillators. A ceramic-based dielectric resonator enclosed in a metallic cavity with an unloaded Q of 13 000 is proposed. The relationship between geometric parameters and resonant frequency is determined. The dielectric puck is then incorporated into multilayer printed circuit boards by using substrate-integrated waveguide techniques. The results show that the resonator resonates at $TE_{01\delta}$ mode with a frequency of 13.3 GHz. Therefore, 13.3 GHz dielectric resonator oscillators with both mechanic and electronic tuning are built. The oscillator includes a pseudomorphic high-electron-mobility transistor low-noise amplifier and an electronic phase shifter. The measured phase noise of the oscillator is −121.7 dBc/Hz at a 10-kHz offset. The calculated and measured phase noise results show a difference of 3 dB.**

***Index Terms*— Dielectric resonators, oscillators, phase noise, substrate-integrated waveguide (SIW), unloaded Q-factor.**

I. Introduction

THE rapid development of wireless communication systems has necessitated the use of high performance and low cost. In transceiver design, the oscillator is a critical component that should have low phase noise in a close carrier and provide a stable frequency source to achieve a high system bit-error rate.

Vitusevich *et al.* [1] recently developed an all-cryogenic low-phase noise sapphire K-band oscillator for satellite communications with an unloaded Q-factor of 1 000 000 and phase noise of –133 dBc/Hz at a 1-kHz offset. Tobar *et al.* [2] presented a compact and high Q-factor sapphire resonator working at TE_{011} mode using a distributed Bragg reflector with an unloaded Q-factor that can reach 70 000. Anstie *et al.* [3] investigated a 50-K dual-mode sapphire oscillator that operates in quasi-orthogonal whispering gallery mode. Ivanov *et al.* [4] demonstrated a sapphire oscillator with a low phase noise of −160 dBc/Hz at 1 kHz offset. However, all these extremely high-Q sapphire resonators require sophisticated temperature compensation systems, thus making their integration into a compact oscillator circuit difficult.

Several low phase noise oscillators using ceramics-based resonators have been recently proposed, but their unloaded Q-factors are lower than those of their sapphire counterparts. An oscillator working at 10 GHz has been proposed in [5]. This oscillator comprises $BaTiO_3$-based resonators with an unloaded Q-factor of approximately 10 000 and phase noise of −135 dBc/Hz at 10-kHz offset. One of the advantages of ceramics-based resonator oscillators is the capability to operate at room temperature. However, integrations with other circuits remain difficult.

Aside from the high Q-factor of a resonator, the low-noise amplifier (LNA) is also an important contributor to the reduction of phase noise of an oscillator [6]. Several sophisticated methods have been proposed for use in an oscillator with a gallium arsenide (GaAs) field-effect transistor (FET)-based LNA, such as interferometric signal processing [4], transposed gain [7], and feedforward techniques [8] to reduce flicker noise.

This paper is an extension of another paper published in APMC2008 [9] and aims to realize tunable microwave low phase noise oscillators using both a metallic cavity through the substrate-integrated waveguide (SIW)-based dielectric resonator technique. First, the relationship between the geometric parameters and resonant frequency of the metallic cavity should be determined. The SIW technique is then adopted to build a dielectric resonator that realizes an integrated low phase noise oscillator to incorporate the dielectric puck into multilayered printed circuit boards (PCBs). The resonant frequency and unloaded Q-factor are numerically characterized. Low flicker-noise amplifiers, high-Q dielectric resonators, an electronic phase shifter, and a directional coupler are also designed to build an oscillator loop for an electronic tunable oscillator, the calculated and measured phase noise of which are given and discussed.

The remainder of this paper is organized as follows. In Section II, high-Q dielectric resonators are realized using a metallic cavity through SIW. The initial dimensions of the cavity are determined based on the calculation of Q factors. In Section III, an LNA and an electronic phase shifter are developed and evaluated. In Section IV, low noise dielectric resonator oscillators are developed, and phase noise is measured and calculated. Conclusions are drawn in Section V.

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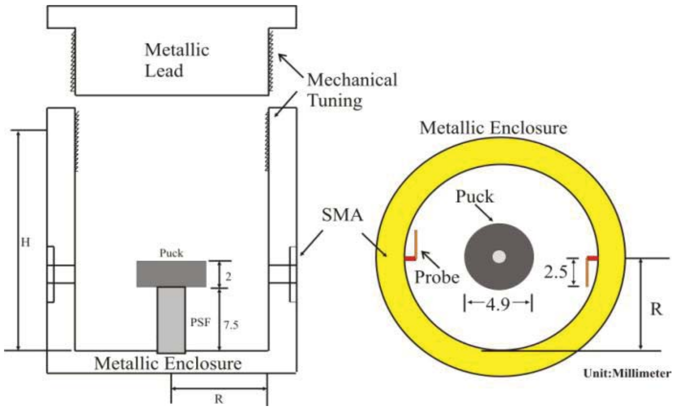

Fig. 1. Geometry of the high-Q dielectric resonator in a metallic cavity (unit: mm).

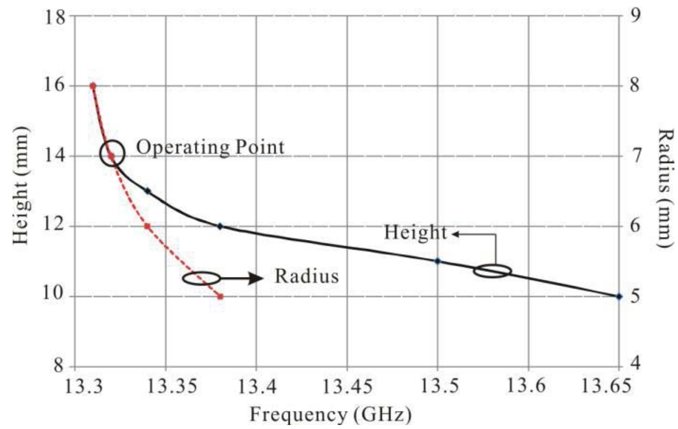

Fig. 2. Relationship of the resonant frequency with the cavity height (H) and radius (R) of the metallic cavity.

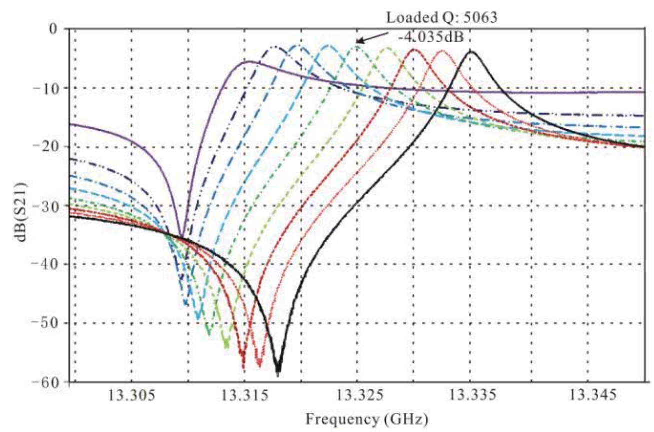

Fig. 3. Measured insertion loss and loaded-Q factor of the metallic cavity-based dielectric resonators with the mechanical frequency tuned by the metallic lead.

II. High-Q Resonator Realization

A. High-Q Dielectric Resonator in a Metallic Cavity

A high-Q dielectric resonator is necessary to establish a low phase noise oscillator. A cylindrical metallic cavity-built dielectric resonator is shown in Fig. 1. A dielectric puck, with $\varepsilon_r = 24$ and an unloaded Q-factor of 13 000, was concentrically mounted into the cavity. The puck bottom was attached using a polysalfone tube with $\varepsilon_r = 3$, which was then glued to the center of the inner cavity. The adhesive was prevented from degrading the Q-factor of the ceramic puck. Thus, a super glue called cyano-acrylate was used. A metallic lead with threads was manufactured for manual mechanical frequency tuning. SMA connectors were screwed into both sides of the cavity. Each end of the SMA connectors was soldered using a coupling wire loop. The insertion loss and loaded-Q factor were set as described in [5] by varying the coupling angle and the length of the loops. When the coupling angle was set as 90°, the loaded-Q factor became almost half of the unloaded one with the insertion loss of the resonator being approximately -6 dB, thus achieving the minimum oscillator phase noise.

The unloaded-Q of the ceramic puck at 13.3 GHz is 13 000, as shown in Fig. 1. However, the inner radius (R) and height (H) of the metallic cavity also affected resonant frequency. A conformal finite-difference time-domain algorithm was developed to analyze the effects of both R and H on the resonant frequency and to determine the initial cavity dimensions [10].

Fig. 2 shows the relationships among cavity height (H), cavity radius (R), and resonant frequency (fres). Given the initial diameter and height of the metallic cavity, the resonant frequencies of the dielectric resonator were calculated. Therefore, $R = 7$ mm and $H = 14$ mm were set to achieve fres $= 13.32$ GHz.

Fig. 3 shows the measured insertion loss and loaded Q-factor of the dielectric resonators with mechanical frequency tuning. A tuning range of 22 MHz was determined, whereas the cavity height varied. The coupling angle of the loops was set to the reverse value. The measured loaded-Q factor was 5000 with an insertion loss of -4 dB. Therefore, the calculated unloaded Q-factor was approximately 13 000.

B. SIW-Built Dielectric Resonator Using Multilayered PCBs

Although the metallic cavity-based dielectric resonator has a high unloaded Q-factor, its integration with other circuits remains difficult. Therefore, we utilized multilayered PCBs to build an SIW-based dielectric resonator, as shown in Fig. 4. A circular resonator with fres $= 13.3$ GHz was designed using an eight-layer PCB. The dielectric puck, surrounded by a metallic via fence, was implemented into the PCB with boards 2 to 4 to form a cavity. The diameter of the vias was 1 mm.

The materials of the multilayered PCBs used to build the SIW-based dielectric resonator were Taconic TSM-30 and Prepregs TPN-30 with the same dielectric constant of 3. The top and cross-section views of the structures are shown in Fig. 4. Two 0.508-mm-thick boards (boards 1 and 4) were placed at the top and bottom of the structure. An unplated cylinder was milled with a radius of 6.9 mm on board 1. Two 1.524-mm-thick boards (boards 2 and 3) were placed in the middle of the structure. The unplated cylinders were milled with radii of 5.4 and 4.9 mm in boards 2 and 3. A small cavity was formed to load a dielectric puck. The radii of

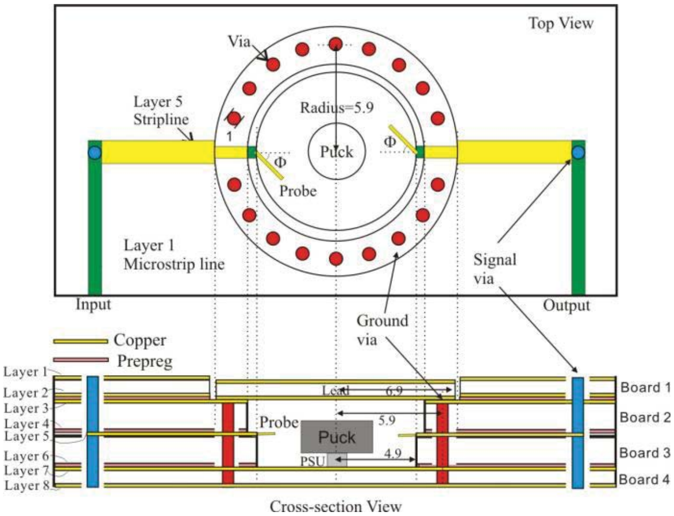

Fig. 4. Resonant frequency and unloaded-Q factor of the SIW-based dielectric resonator as a function of the radius R.

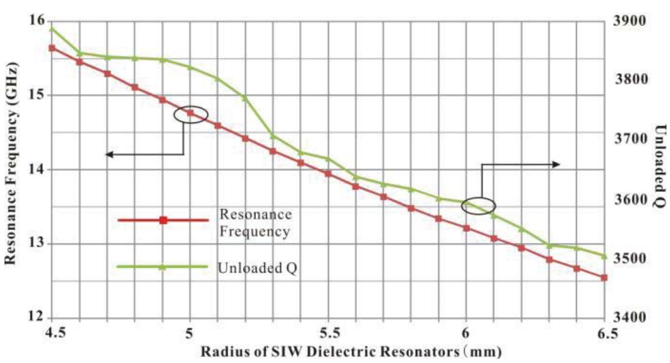

Fig. 5. Resonant frequency and the unloaded-Q factor of the SIW-based dielectric resonator as a function of the radius R.

boards 2 and 3 determined the resonant frequency of the SIW-based dielectric resonators. Therefore, a full-wave electromagnetic (EM) simulator HFSS was used to characterize the resonant frequency and unloaded Q-factor.

Fig. 5 shows the values of fres and unloaded-Q for different radii of the SIW. The resonant frequency was 13.3 GHz when $R = 5.9$ mm. Under such condition, the unloaded Q-factor was approximately 3600, 73.4% lower than that of the original ceramic puck case.

The manufacturing processes of SIW-based dielectric resonators are described as follows.

The structure has eight layers. Layers 1 and 5 are first etched with only microstrip lines and striplines left, respectively. Layers 4 and 6 are etched without copper. Boards 2, 3, and 4 are then bonded using Prepregs TPN-30. Plated-through ground holes are drilled from Layers 3 to 8 to form a circular via fence as an SIW. The radius of the vias is 0.5 mm. Board 1 is then bonded with boards 2 to 4 using Prepregs TPN-30. Two plated-through signal holes from layers 1 to 8 are drilled at the connections between the microstrip lines in layer 1 and the striplines in layer 5. A cylindrical lead using a 0.508-mm PCB board with double-sided copper is soldered in layer 3.

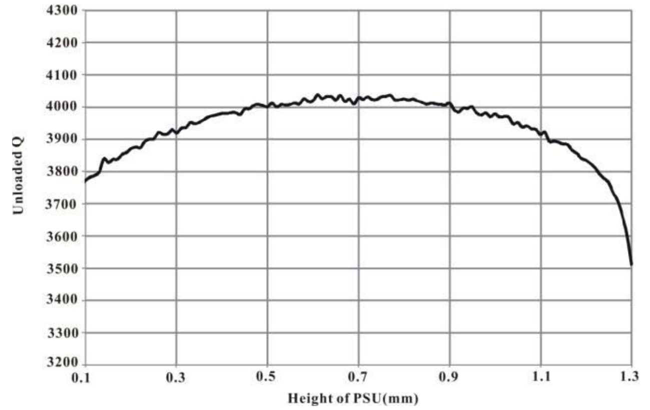

Fig. 6. Simulated unloaded Q-factor as a function of the height of the puck support PSU.

One dielectric puck with unloaded $Q = 13\,000$, height $=$ 2 mm, and radius $= 2.45$ mm is concentrically attached with a support (PSU) to board 4. Two coupling wire loops are soldered at each side of layer 5. The -6 dB insertion loss and loaded Q factor of the SIW-based dielectric resonators are then tuned by changing the angles of the coupling wire loops.

The unloaded Q-factor of the SIW-based dielectric resonator is calculated by

$$\begin{aligned} 1/Q_u &= 1/Q_c + 1/Q_d + 1/Q_{\text{leak}} \\ &= 1/Q_{\text{metal}} + 1/Q_{\text{puck}} + 1/Q_{\text{leak}} + 1/Q_{\text{sub}} \end{aligned} \tag{1}$$

where Q_c, Q_d, Q_{leak}, Q_{metal}, Q_{puck}, and Q_{sub} are the unloaded Q-factors corresponding to the conductive loss of PCB, dielectrics loss of PCB, leakage loss, metal plane loss, dielectric puck loss, and substrate loss, respectively. When the distance between the two vias (P_{via}) in the SIW is smaller than two-fold the via diameter, leakage loss is negligible [11], and Q_{leak} becomes infinity. The Q_{sub} could also be neglected because the surrounding materials of the dielectric resonators are mostly air-filling. The Q-factor Q_{metal} is given in [15]. Therefore, (1) is written as

$$Q_u \approx 1/(1/Q_{\text{metal}} + 1/Q_{\text{puck}}) = 4074. \tag{2}$$

Based on (2), the unloaded Q-factor of the SIW-based dielectric resonator is mainly determined by Q_{metal} and decreases with decreasing distance between the puck and the metal plane. By increasing the height between the dielectric puck and the metal plane, a larger Q_u can be obtained. Fig. 6 shows the unloaded Q-factor as a function of the height of puck support (PSU), which is optimized when the height of PSU is set to 0.5 mm. Under such condition, the unloaded Q-factor is approximately 4000, which agrees well with the calculated value.

Upon the determination of the unloaded Q-factor of the SIW-based dielectric resonator, the loaded Q-factor can be set by varying the wire loop angle (Φ), as described in [5]. Given that the angle Φ is nearly equal to $90°$, $Q_L/Q_0 = -0.5$, and insertion loss $S_{21} = -6$ dB. Fig. 7 shows the frequency responses of the dielectric resonator, where no resonance peak is observed below 13.3 GHz. The loaded

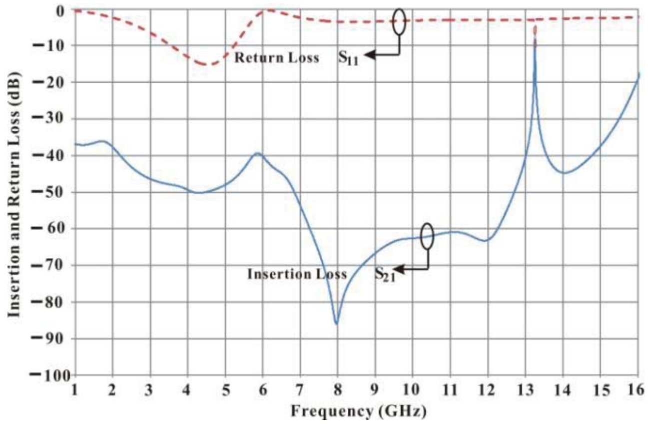

Fig. 7. Insertion and return losses of the SIW-based dielectric resonator.

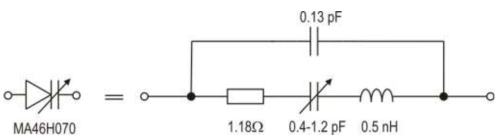

Fig. 8. Model of a packaged Macom varactor diode (MA46H070).

Q-factor is approximately 1900 with an insertion loss of -7 dB. Therefore, the unloaded Q-factor of the SIW dielectric resonator is approximately 3500.

III. LNA and Phase-Shifter Realization

A. Low-Noise Amplifier

The insertion loss of the dielectric resonator was set at – approximately -6 dB. To achieve the best phase noise performance, an LNA was designed to provide sufficient open-loop gain to compensate for all losses caused by the dielectric resonator, coupler, phase shifter, and loop transmission lines. To achieve the desired phase noise level, the transistors should also have a low-noise value and low flicker noise corner. Therefore, an Avago GaAs pseudomorphic high electron mobility transistor (PHEMT) ATF-36077 was used with a gain (S_{21}) of 7.5 dB at 13.3 GHz and a return loss (S_{11}) optimized at -13 dB.

B. Phase Shifter

Narrow-band tuning is typically achieved in the DRO so that the device can be implemented into the phase-locked loop. However, the tuning function should not negatively affect the phase noise of an oscillator. The tuning function can be realized in two ways: by integrating the tuning circuit into the resonator and by introducing a phase shifter into the oscillating loop. Therefore, an electric phase shifter network has to be incorporated into the delay line of an oscillator if the tuning element cannot be integrated into a tunable DRO of the resonator. This process enables the resonator and tuning elements to be optimized separately [12].

A varactor model, as shown in Fig. 8, is needed in the design of a tuning element. This model comprises a variable series capacitance, a parasitic series inductance, a series resistance, and a parallel capacitance. The variable capacitance ranges

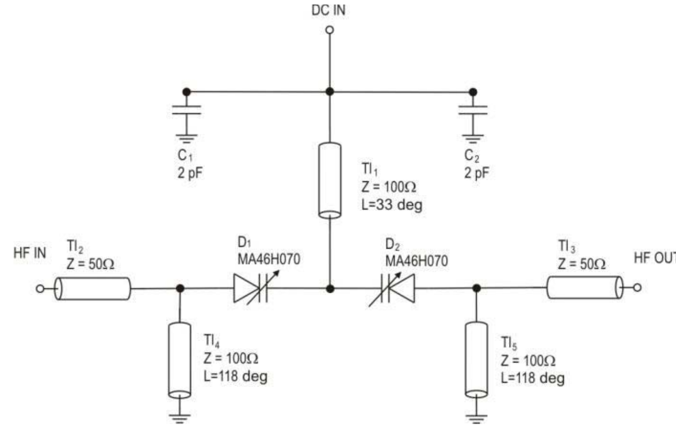

Fig. 9. Schematic of an electronic phase shifter.

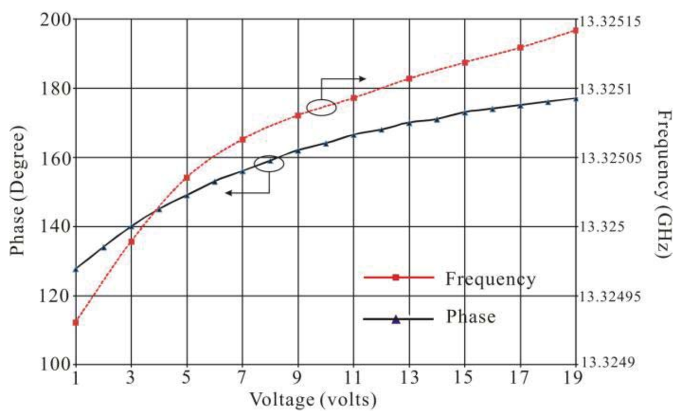

Fig. 10. Measured insertion loss and phase shift as a function of applied voltage.

from 0.4 to 1.2 pF. The series resistance is calculated to be 1.18 Ω, given that the datasheet provides a Q-factor of 5000 [13].

The structure of an electric phase shifter is shown in Fig. 9. First, a lumped fifth order high-pass filter was designed and analyzed. The capacitances were then replaced by varactor diodes. The shunt microstrip lines TL_1, TL_2, and TL_3 were used as inductances. Fig. 10 shows the measured phase shift and tuning frequency as a function of applied voltage. The phase shift range was approximately 50°, and the frequency tuning range was approximately 200 kHz. The insertion loss was approximately 3 dB, a value that is higher than expected because the Q-factor of the varactor diode dropped with increasing frequency.

IV. Discussion of Calculated and Measured Phase Noise

The structure of the electronic tunable dielectric resonator oscillator is shown in Fig. 11. The oscillator comprises a high-Q dielectric resonator, two cascade LNAs, a 10-dB direction coupler, and an electronic phase shifter. The output coupler is placed between the LNA and the high-Q dielectric resonator to obtain the output oscillating signal sample and to measure the power level at the LNA output (P_{AVO}). The electronic phase shifter is placed at the input of the LNA and at the output of the high-Q dielectric resonator, which aids in

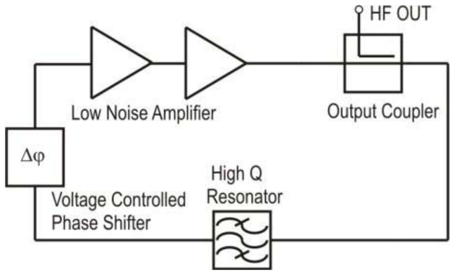

Fig. 11. Diagram of the low-noise dielectric resonator oscillator with the tuning function.

eliminating the nonlinear effects of the varactor, as described in [14].

The phase noise of an oscillator was first derived by Leeson. However, the model did not consider either the effects of the coupler or the noise floor of the LNA. Everard [15] optimized Leeson's model to achieve the minimum phase noise through (3) and (4)

$$L_{\mathrm{FM}} = \frac{\mathrm{FkT}(1+\mathrm{f_c}/\Delta\mathrm{f})}{8Q_0^2(Q_L/Q_0)^2(1-Q_L/Q_0)^2P_{\mathrm{AVO}}}(f_0/\Delta f)^2. \quad (3)$$

When $Q_L/Q_0 = 1/2$ and the insertion loss of the resonator is set as -6 dB, the minimum phase noise is determined by

$$L_{\mathrm{FM}} = 2\mathrm{FkT}(1+f_c/\Delta f)(f_0/\Delta f)^2/(Q_0^2P_{\mathrm{AVO}}). \quad (4)$$

Fig. 11 shows that the noise at the output of the coupler transferring into the oscillator loop should also be considered and can be presented as $\mathrm{FkT}/\mathrm{C}_0P_{\mathrm{AVO}}$, which correlates with coupling ratio of the directional coupler. The noise floor of the LNA can be presented as $\mathrm{FkT}/P_{\mathrm{AVO}}$. The value of the noise figure should also include the LNA and insertion loss of the phase shifter because the latter is included between the input of the amplifier and the output of the resonator. The total phase noise of an oscillator including a coupler and a phase shifter is

$$L_{\mathrm{FM\ Theoretical}} = 10\cdot\log\left[\frac{2\mathrm{FkT}(1+\mathrm{f_c}/\Delta\mathrm{f})}{Q_0^2P_{\mathrm{AVO}}}+\frac{\mathrm{FkT}}{C_0P_{\mathrm{AVO}}}+\frac{\mathrm{FkT}}{P_{\mathrm{AVO}}}\right] \quad (5)$$

where k is the Boltzman's constant, and $T = 290$ K. The loaded-Q factor (Q_0) is approximately 13 000 with $S_{21} = -4$ dB. Thus, the unloaded-Q factor (Q_L) is 5000. The measured power available at the output of the cascaded amplifiers P_{AVO} is 8 dBm. C_0 is the coupler ratio (10 dB) with respect to the output of the coupler. The parameter f is the operating frequency, whereas Δf is the offset frequency. f_C is the flicker noise corner of the PHEMT transistor [18].

Fig. 12 shows the phase noise measurement system. The details of the measurements process include the following steps. The HP8662 signal synthesizer generates the reference oscillator signal at 160 MHz, which is divided by 16, amplified to produce a power level of 0 dBm, and then connected to the input of the phase noise carrier test set (HP11729). A 0 to 40 dB attenuator is added for calibration. The attenuator is set to 0 dB in the measurement mode and to 40 dB in the calibration mode to measure the beat note. Using the divider ensures that the noise floor of the reference signal generator

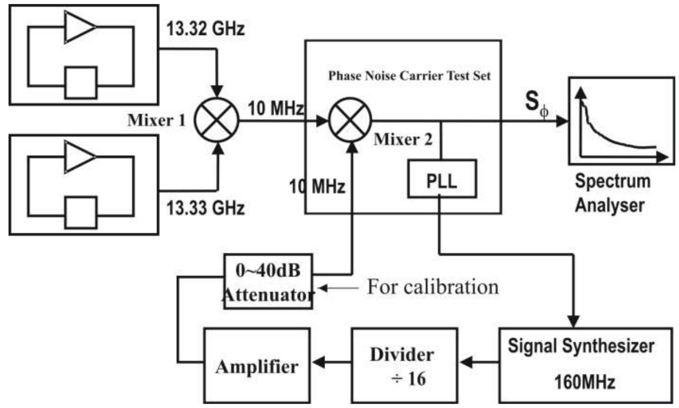

Fig. 12. Phase noise measurement system.

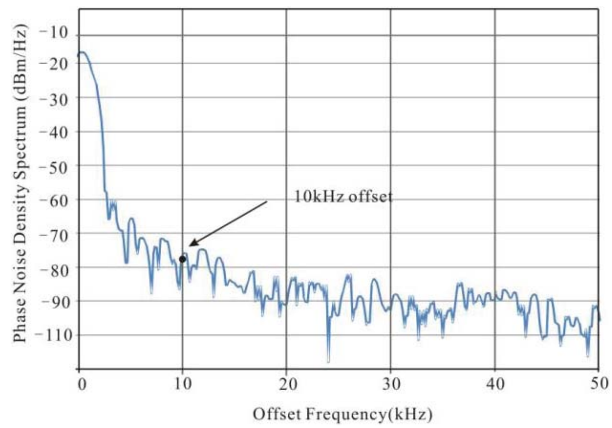

Fig. 13. Measurements of dielectric resonator oscillator as a function of frequency.

(HP8662) is close to the phase noise of the DRO. The noise floor of the divider at 10 kHz is -140 dBc. Therefore, the noise floor of the system is set –to -140 dBc/Hz at a 10-kHz offset. Notably, HP8662 has the best phase noise from 120 to 160 MHz.

Two identical DROs with an offset of 10 MHz were integrated. One of the dielectric resonators was mechanically tuned to increase the operating frequency described in Section II.

The mixed signal with a 10-MHz offset was then connected to the mixer of the carrier test HP11729.

Fig. 13 shows the measured phase noise density spectrum of the dielectric resonator oscillator displayed in the spectrum analyzer of the phase noise measurement system. The offset frequency ranged from 1 to 50 kHz.

As an example, the phase noise measurement of the DROs at the 10-kHz offset can be calculated as

$$\begin{aligned} L_{\mathrm{FM}} &= \frac{1}{2}S_\phi(f) = \frac{1}{2}\left(\frac{\Delta V_{\mathrm{RMS}}^2}{K_\phi^2}\right) \\ &= \frac{1}{2}\left(\frac{\Delta V_{\mathrm{RMS}}}{V_{B\,\mathrm{Peak}}}\right)^2 = \frac{1}{4}\left(\frac{\Delta V_{\mathrm{RMS}}}{V_{\mathrm{BRMS}}}\right)^2. \end{aligned} \quad (6)$$

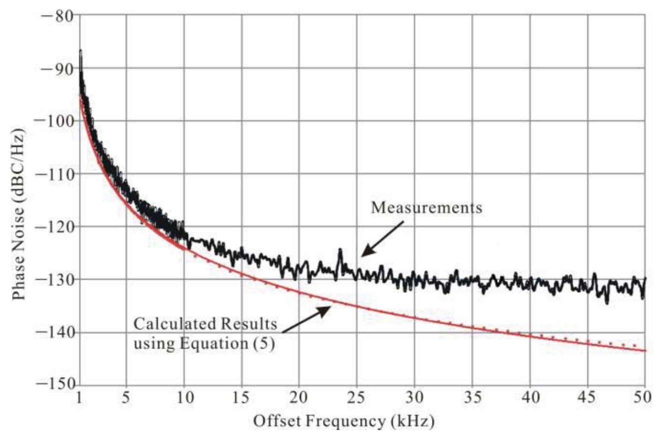

Fig. 14. Comparisons of the phase noise between measurements and calculated results.

TABLE I
MEASURED AND CALCULATED PHASE NOISE OF A DIELECTRIC RESONATOR OSCILLATOR

Phase Noise at Offset	Measurements dbc/Hz	Calculated Results Using Eq. (9) dBc/Hz
1 kHz	−91.8	−95.2
5 kHz	−113.1	−115.7
10 kHz	−121.7	−124
15 kHz	−125.4	−129.2
20 kHz	−129.2	−132

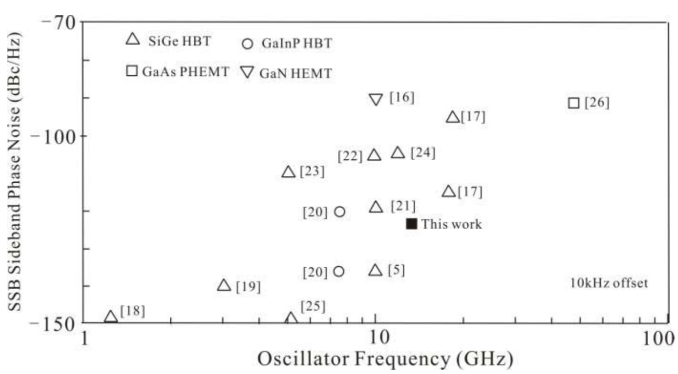

Fig. 15. Summary of previously reported DRO phase noise performance.

Equation (6) could be converted to dB and can be directly used for the measurements

$$\begin{aligned} &L_{\mathrm{FM}}[\mathrm{dBc/Hz}] \\ &= \Delta V_{\mathrm{RMS}}^2[\mathrm{dBm/Hz}] - V_{\mathrm{BRMS}}^2[\mathrm{dBm}] - 6\ \mathrm{dB} - 40\ \mathrm{dB} \\ &= -78.7\ \mathrm{dBm/Hz} - (-6\ \mathrm{dBm}) - 6\ \mathrm{dB} - 40\ \mathrm{dB} - 3\ \mathrm{dB} \\ &= -121.7\ \mathrm{dBc/Hz} \end{aligned} \tag{7}$$

where S_Φ is the spectral power density of phase fluctuations; K_Φ is the phase detector constant, which is equal to $V_{B\mathrm{Peak}}$ for small phase deviation.

$\Delta V_{\mathrm{RMS}}^2$ is the phase noise density spectrum, which is displayed on the spectrum analyzer at the 10-kHz offset, and $V_{B\,\mathrm{Peak}}$ is the peak voltage of beat note and is converted to $V_{B\,\mathrm{RMS}}$. $V_{B\,\mathrm{RMS}}$ is 6 dBm, as displayed on the spectrum analyzer at the calibration mode, where 6 dB is derived from 1/4, which is converted to dB; 40 dB is the attenuation in the calibration mode, and 3 dB is subtracted to derive the phase noise of a single oscillator.

The phase noise of the DROs at an offset frequency ranging from 1 to 20 kHz was measured using (6). Fig. 14 shows the phase noise comparisons between the measured data and the data calculated using (5). Table I summarizes the results. The measured and calculated phase noises were closer from 1 to 20 kHz within 3 dB. However, the measured phase noise was limited by the noise floor of the testing system above 20 kHz because of the noise floor of the measurement system. Fig. 15 summarizes the phase noise (at 10 kHz offset) reported for the microwave and millimeter wave DROs [5], [16]–[26].

V. CONCLUSION

In this paper, a metallic enclosure and a multilayer SIW-based dielectric resonator were realized and investigated in detail. The metallic cavity loaded with a dielectric resonator and an SIW-based dielectric resonator had a Q-factor of 13 000 and 3600, respectively. However, the latter can be easily integrated with other circuits. A low-noise PHEMT-based amplifier and an electric phase shifter were designed and used to sample the oscillating signal. A modified phase noise model, including the flicker noise corner, was presented to predict the phase noise performance of the dielectric resonator oscillator accurately. The measured and calculated phase noise of the dielectric resonator oscillator was approximately −121.7 dBc/Hz at 10 kHz offset.

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